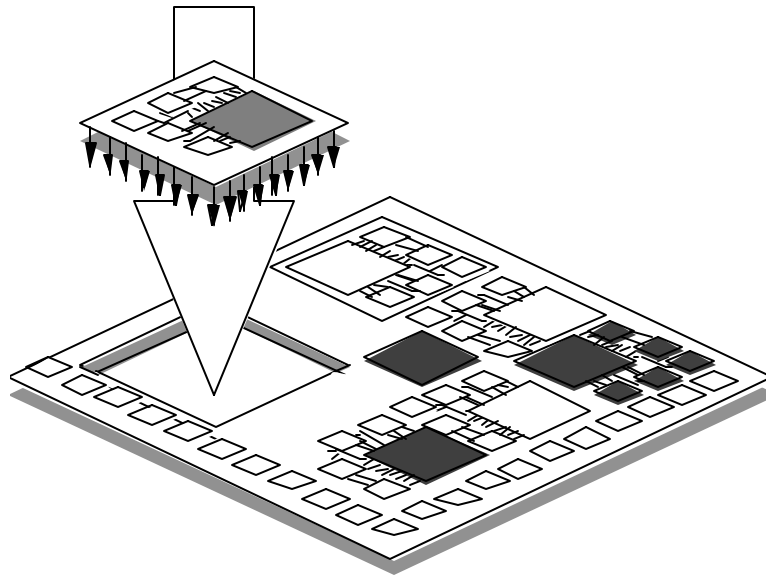


VSI Alliance™
Analog/Mixed-Signal VSI Extension
Specification Version 2.2
(AMS 1 2.2)

Analog/Mixed-Signal
Development Working Group

February 2001



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The participants include analog/mixed-signal designers, test engineers, mixed-signal VC providers, system integrators, EDA developers, and ASIC designers.

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1. Overview

1.1 Scope

The scope of this document is to specify deliverables, their associated design guidelines, and data formats to facilitate the test, exchange, and integration of process specific (“hard”) mixed-signal virtual components. These components target largely digital system chip applications.

This document also provides a detailed deliverables list of models to assist the exchange, integration, and verification of process specific (“hard”) mixed-signal virtual components.

The “field of use” for VSIA standard data formats is defined as creating, defining, exchanging, and integrating descriptions of virtual components (VCs) of integrated circuits.

1.2 Referenced Intellectual Property

This specification references a number of data formats, including:

- VC Hspice: VC Hspice 1.0a
 - Owner: Avant! Corporation
 - Status: Licensed through Technology Contribution Agreement
 - <http://www.vsi.org>
- VC LEF: VC LEF 5.1
 - Owner: Cadence Design Systems, Inc.
 - Status: Licensed through Technology Contribution Agreement
 - <http://www.vsi.org>
- GDSII: GDSII Stream Format 6.0.0
 - Owner: Cadence Design Systems, Inc.
 - Status: Licensed through Technology Contribution Agreement
 - <http://www.vsi.org>
- Verilog: IEEE 1364-1995
 - Owner: IEEE
 - Status: Accredited standard
 - <http://standards.ieee.org/faqs/order.html>
- VHDL: IEEE 1076-1987
 - Owner: IEEE
 - Status: Accredited standard
 - <http://standards.ieee.org/faqs/order.html>
- Verilog-AMS: Verilog-AMS Version 2.0¹
 - Owner: OVI
 - Status: Under Development (Version 1.3 is an approved standard)
 - <http://www.ovi.org/>
- VHDL-AMS: IEEE 1076.1-1999
 - Owner: IEEE
 - Status: Accredited standard
 - <http://standards.ieee.org/faqs/order.html>

¹It is anticipated that the tools that will support Verilog-AMS will be based on the 2.0 version.

- Open Library API (OLA)
 - Owner: OLA task force
 - Status: Under Development
 - <http://www.si2.org/ola>
- SPEF: IEEE P1481, 1998
 - Owner: IEEE
 - Status: IEEE Ballot Standard
 - <http://vhdl.org/vi/dpc/dpc-pandc/>

1.3 Assumptions

The following assumptions attempt to bound the problem, so an analog VSI extension is feasible in the short term. The assumptions are divided into three categories - VC properties, technology, and usage. The topics outside of these bounds are considered too complex for the first pass at the analog VSI extension.

1.3.1 VC Properties

The following assumptions are made about the properties of the virtual components addressed by the analog VSI extension:

- Only blocks with complex functionality, such as PLL, A/D, D/A, are considered. Since the creation, packaging, and integration (usage) of a block in VSI form will take significant time and effort, each block must be large enough to justify the time and effort invested. The smaller components, such as Voltage Controlled Oscillator (VCO), Charge Pump (CP), Operational Transconductance Amplifier (OTA), do not interest a VC integrator, just as a VC integrator is not interested in buying a NAND gate.
- Each virtual component will have a robust interface and is easily separable from its environment. Thus, components that require a tight feedback loop to work together for better functionality or performance are considered one VC, which is separable from the rest of the system. The interface of the combined VC will be self-contained.
- In general, VC authors should not take advantage of process tracking and other correlation effects that exist on the same IC between different analog blocks. In other words, each analog/mixed-signal VC should be designed independently. For example, block A should not take advantage of the fact that V_t will be correlated into block B, even though they exist on the same IC.
- A mixed-signal component can be tested using established digital test methodology as a basis, and it will not interfere with digital test (e.g. IDDQ).

1.3.2 Technology

The following assumptions are made about the implementation of analog/mixed-signal VCs from a technology or process viewpoint:

- The VCs are targeted at standard CMOS processes, requiring a minimum number of or no extra process steps.
- The VCs will be process targeted (hard) blocks, i.e. VCs will be in layout form, targeted to a specific process. The process variation information is considered only as it applies to one process. The change in process over time will be accounted for.
- The issues related to process design rules, interfaces to manufacturing, and so forth are outside the scope of this document.
- This document focuses on issues that clearly arise because of the change from board to silicon. If a problem already exists in the board integration world, this document does not focus on it.

1.3.3 Usage

The following assumptions are made about the use of VCs by an integrator who designs “System-on-a-chip”:

- The “System-on-a-chip” device is primarily digital logic with a small amount of analog components. For example, a system could be composed of a DSP core, RAM cache, μ P cores, A/D, and D/A converters. A system is considered an integration of an existing solution based on one or more boards.

- Systems will be part of consumer applications driven by time-to-market (TTM), low cost, high volume considerations.
- Schematics of the VCs will not be required by the VC integrator to protect the author's IP as well as avoid schematic format delivery problems. In general, an attempt will be made to hide the internal structure or detail of the VC. This is similar to using digital "hard" blocks without RTL code.
- Digital VCs will be used when digital VSI is applicable. If the digital and analog blocks can be separated easily in a true "mixed-signal" block, then the digital VCs will follow the digital VSI rules and can be shipped as soft, firm, or hard.
- "System-on-a-chip" designers are willing to give up performance in the selection of the analog/mixed-signal virtual components for improved ease in integrating them.
- Applications engineering support is available just as there is such support for the IC delivery. It is in the interest of the author to make the integrator successful and to provide necessary application support to achieve mutual success.
- As the VSI standard evolves, it will address issues with BiCMOS and RF technologies, soft and firm blocks, schematics, and so forth for analog VSI components.

1.4 Methodology Overview

This section describes the flow of data, documents, and other information between the VC creator (also called the provider or author in this document) and the VC integrator (also called the user or consumer). Figure 1: Analog VSI Extension Flow shows the flow applicable to the analog VSI extension with the assumptions made earlier. Figure 1: Analog VSI Extension Flow is derived from Figure 4: Virtual Component Design Methodology, in the *VSI Alliance Architecture Document, Version 1.0*. The arrows represent places where the VC provider will hand over information to the VC integrator in the basic VC integrator flow as shown in the *VSI Alliance Architecture Document*.

The flow is intended to concisely define the deliverables a VC provider delivers to a VC integrator. This document hopes to facilitate the process and replace 80-90% of the interaction required for the transfer of VCs by providing answers to many frequently asked questions. However, it is inevitable that additional communication (e.g. application engineering support) will be required outside the analog VSI extension.

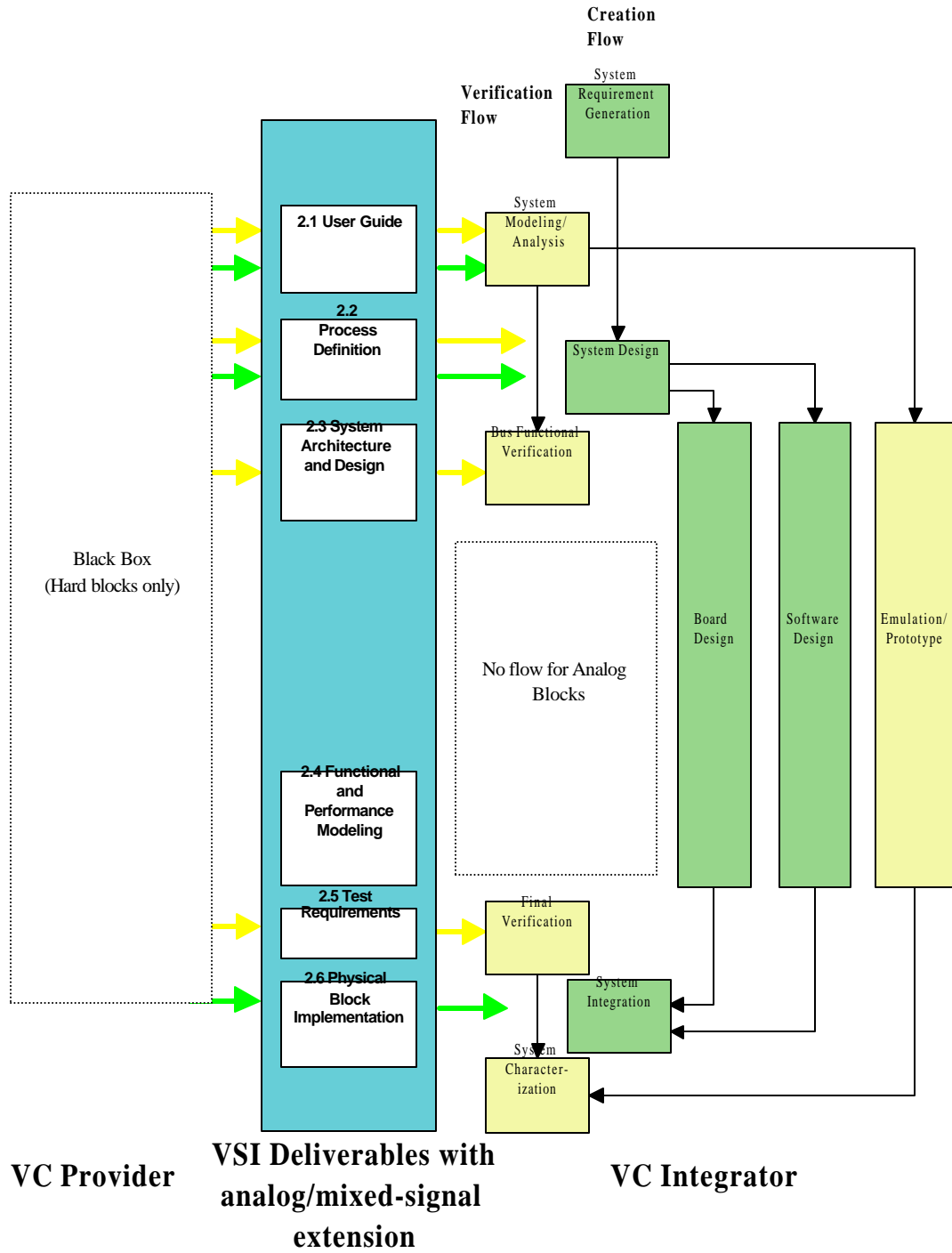


Figure 1: Analog VSI Extension Flow

The provider/integrator methodology described in this document for analog blocks is significantly simpler than for digital blocks, because only hard blocks are considered in this document. Therefore, there are only outputs at the top (user guide and system architecture/design documents) and at the bottom (test and physical) in the provider flow. There are no soft blocks or firm blocks, so there are no outputs in the middle to provide any intermediate form to the VC integrator. There is also no flow in the middle on the integration side, since the VC providers only distribute hard blocks. Finally, the methodology for designing the actual analog/mixed-signal virtual component is left as a “black box” so VC providers are free to choose their own preferred VC design methodology.

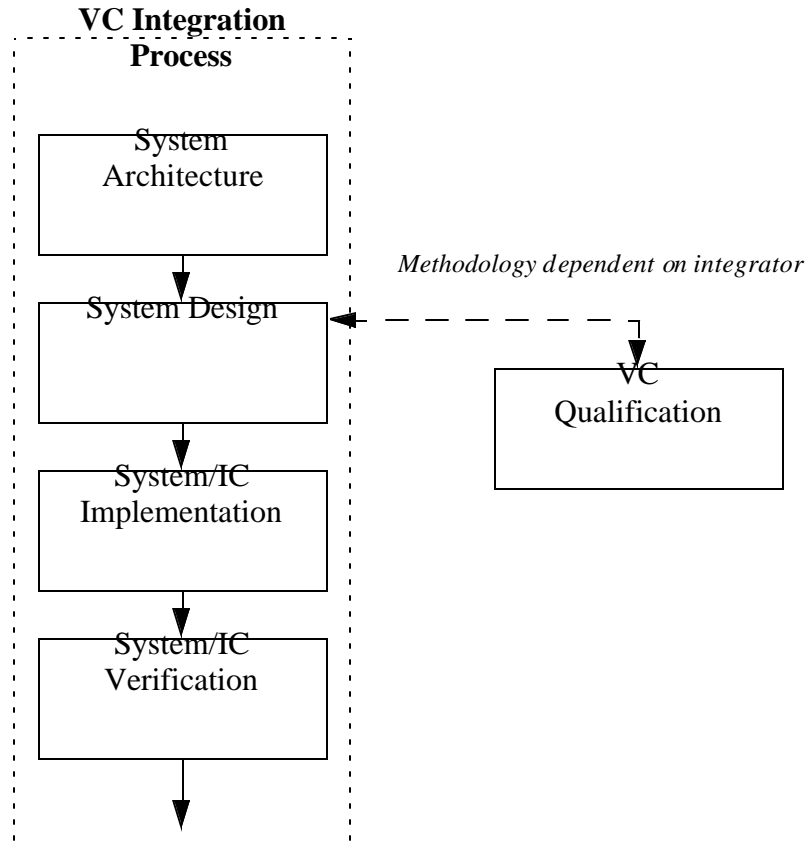


Figure 2: Analog/Mixed-Signal Virtual Component Design Methodology

A generic design methodology as shown in Figure 2: Analog/Mixed-Signal Virtual Component Design Methodology was used in developing the deliverables list. The VC integration process for all VCs (digital, A/MS, etc.) is illustrated. The steps on the left are the absolutely necessary steps for VC integration. The VC Qualification step (on the right) is an optional step for the VC integrator who wants more assurances of the VC that is being integrated.

The assumption is that this is the typical integrator’s digital design process. This document provides the suggested modeling deliverables for A/MS VCs for each of the steps shown in the figure. In determining the deliverables for each step, it was also recognized that certain models may be used in more than one of the steps shown in the figure. The intent is to make certain that all necessary models have been specified, not to absolutely associate them with a particular step.

We are proposing models in the system space, and, because SOC is still being defined, we believe that the functional and performance models at lower levels of details (i.e. in the implementation/verification space) are better understood. We have, therefore, concentrated on the implementation/verification level. We have also chosen not to attempt to define more crisply exactly what is meant by “system” as there are other working groups currently addressing this problem. Instead, we decided to adhere to the definition as set out in the *VSI Alliance Architecture Document*.

1.5 VSI Deliverables

To improve communication and ensure sufficient information at the integration stage, this section identifies a number of deliverable items that can be provided by the VC developer to the VC integrator. If a reference document is noted in the table, additional information about that deliverable is available in the referenced document. Often, the reference is to a digital equivalent model. The description found in Section 2 contains information on how the deliverable may have been modified to accommodate additional A/MS concerns.

The following list describes the columns in Table 1 and the keywords used in the columns.

Section	References the document section that discusses the deliverable.
Deliverable	Describes the deliverable.
VSIA Endorsed Formats	Lists the formats being developed as standards, meeting the VSIA DWG's requirements.
VSIA Specified Formats	Lists currently available open formats that have been approved by the respective VSIA DWG.
A/MS Hard	Describes the applicability of the deliverable for the A/MS "hard" VC.
M	Denotes Mandatory. Mandatory is a deliverable required to make most chip designs workable that use the particular type of VC denoted by the column it resides in.
CM	Denotes Conditionally Mandatory (requirement is based on application).
R	Denotes Recommended. Recommended is a deliverable to improve the design time, quality or accuracy for most chip designs that use the particular "hardness" of a VC denoted by the column it resides in.
CR	Denotes Conditionally Recommended (requirement is based on application). For CM and CR, conditional comments should identify a class of designs, VCs or chips containing VCs, where this deliverable is applicable if the defined condition is met. Conditions are sufficiently described to delineate the class of designs.
Comments	Comments supply clarifying information. The specific conditions necessary to meet a Conditionally Mandatory or a Conditionally Recommended must be described within the Comments section for each conditionally assigned deliverable. This column is also used by VC providers for comments or for references to comments in the Comment section of a compliance report. If there is lack of space in this column, comments can be appended.
TBD	To be determined.

IMPORTANT: Verification test bench documentation and model validation documentation must be supplied for all models which are delivered.

Table 1: VSIA Data Deliverables

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Format(s)	A/MS Hard	Comments
2.1	User Guide				
2.1.1	Specification				
2.1.1.1	System Description		document	M	
2.1.1.2	Block Diagram		document	M	
2.1.1.3	Register Description		document	CM	If there are registers present, this deliverable is M.
2.1.1.4	Timing Diagram		document	M, R	If there is digital I/O, this deliverable is M. If there is analog I/O, this deliverable is R.
2.1.1.5	Clock Distribution		document	CM	If there is a clock, this deliverable is M.
2.1.1.6	Bus Interfaces & I/O Configs		document	M	
2.1.1.7	Test Description Summary		document	M	
2.1.1.8	Integration Requirements		document	R	
2.1.1.9	Schematic Block Diagrams		document	R	
2.1.1.10	Operating Modes		document	M	
2.1.1.11	Bias Supply Management		document	CM	If there is a bias supply, this deliverable is M.
2.1.1.12	Operating ranges		document	M	
2.1.1.13	Power Supplies		document	M	
2.1.1.14	Electrical Specifications		document	M	
2.1.1.15	Bonding Pad Requirements		document	CM	If special pads are required, this deliverable is M.
2.1.2	Claims and Assumptions		document	M	
2.1.3	Verification of Claims		document	M	
2.1.4	Version History		document	M	
2.1.5	Known Bugs		document	M	
2.1.6	Application Notes		document	R	
2.2	Process Definition				

Table 1: VSIA Data Deliverables (Continued)

Section	Deliverable	VSIA		A/MS Hard	Comments
		Endorsed Formats	Specified Format(s)		
2.2.1	Process Requirements		document	M	
2.2.2	Process Tolerances		document	M	
2.2.3	Process Sensitivities		document	R	
2.2.4	Process Design Rule Exceptions		document	CM	If the design rules are intentionally violated, this deliverable is M.
2.2.5	VC Processing History/ Portability		document	R	
2.3	System Architecture and Design				
2.3.1	Algorithmic Level Model		TBD- electronic format pertaining to the tool	R	VSIA may define a more specific format or set of formats at a later time.
2.3.2	System Evaluation Model / Behavioral Model		TBD- electronic format pertaining to the tool	R	VSIA may define a more specific format or set of formats at a later time.
2.3.3	Bonded Out VC/ Prototype		Packaged Integrated Circuit, document	R	
2.4	Functional and Performance Modeling				
2.4.1	Digital Placeholder ("Dummy") Model		Verilog, VHDL	R	
2.4.2	Functional/Timing Digital Simulation Model		Verilog, VHDL	R	
2.4.3	Digital Timing Model for Static Timing	OLA		R	
2.4.4	Bus Functional Model (for digital interfaces)		TBD	R	Format to be determined by the VSIA SLD Interface subgroup.
2.4.5	Peripheral Interconnect Model (for digital interfaces)		SPEF	CM	If there is a measurable level of interconnect between the I/O ports and the internal gates of the VC, this deliverable is M.
2.4.6	Electrical Port Models				

Table 1: VSIA Data Deliverables (Continued)

Section	Deliverable	VSIA Endorsed Formats	VSIA Specified Format(s)	A/MS Hard	Comments
2.4.6.1	Digital Electrical Port Model (device level interface netlist)		VC Hspice	R	
2.4.6.2	Analog Electrical Port Model		VC Hspice	R	
2.4.7	Block level HDL Simulation Model	Verilog- AMS, VHDL- AMS		R	
2.4.8	Detailed Transistor/Gate Level Schematics		any suitable format	CR	If the VC provider agrees to release this deliverable, it is R. There may be IP Protection issues requiring discussion between the VC provider and the VC integrator.
2.4.9	Circuit Level Simulation Netlist		VC Hspice	CR	If the VC provider agrees to release this deliverable, it is R. There may be IP Protection issues requiring discussion between the VC provider and the VC integrator.
2.5	Test Support				
2.5.1	Signal Requirements		document	M	
2.5.2	Test Requirements		document	M	
2.6	Physical Block Implementation				
2.6.1	Detailed Physical Block Description		GDSII-Stream	M	
2.6.1.1	Layer Mapping Table		document	M	
2.6.2	Pin List/Pin Placement		VC LEF	M	
2.6.3	Routing Obstructions		VC LEF	M	
2.6.4	Footprint		VC LEF	M	
2.6.5	Power and Ground		VC LEF	M	
2.6.6	Layer Mapping Table		document	M	
2.6.7	Physical Netlist		VC Hspice	CM	If layout versus schematic is required by the VC integrator, this deliverable is M.
2.6.8	General Physical Rules				

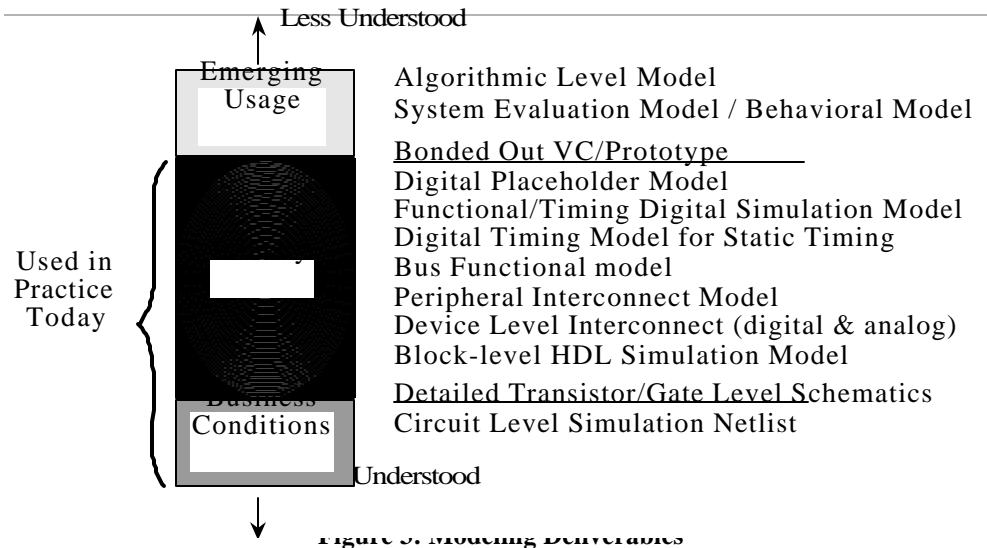
Table 1: VSIA Data Deliverables (Continued)

Section	Deliverable	VSIA		A/MS Hard	Comments
		Endorsed Formats	Specified Format(s)		
2.6.8.1	Physical Isolation Specification		document	M	
2.6.9	Placement Specifications				
2.6.9.1	Placement Constraints		document	M	
2.6.9.2	Proximity Effects		document	M	
2.6.10	Interconnect Specifications				
2.6.10.1	Special Hookup Guidelines		document	M	
2.6.10.2	Routing Constraints		document	M	
2.6.10.3	Special Pin Requirements		document	M	
2.6.10.4	Additional Power, Ground, and Substrate Interconnect Constraints		document	M	
2.6.11	Substrate Sensitivity/Constraints		document	R	

Note With respect to compliance, all lists of formats for a given category and deliverable may be viewed as OR of the individual formats. That is, any of the listed formats may be used to satisfy the deliverable. If AND is intended for any list of formats, this requirement must be indicated in the Comments section and prior to the Specification’s deliverables summary.

1.5.1 Modeling Deliverables

The modeling deliverables are divided into three categories: Primary, Dependent on Business Conditions, and Emerging Usage. Figure 3: Modeling Deliverables illustrates these categories. The Primary category is the focus of the modeling deliverables in this document. These are modeling types that are beginning to be used in practice today. The Dependent on Business category includes deliverables that are used today but are subject to negotiation between the VC provider and VC integrator. The Emerging Usage category provides placeholders for emerging models used with A/MS VCs.



These items are vertically ordered from the highest level of abstraction on the top to the lowest level of abstraction on the bottom. However, the best understood description tends to go from the bottom to the highest. Emerging Usage also lists some design practices that are still in flux. Algorithmic Level Models and System Evaluation Models are very dependent on the system integrator and the VC in question; these models may or may not require that the VC provider develop them. The intent of proposing a category for emerging deliverables is twofold: (1) if it is provided in the future, this specification has a placeholder for it, and (2) it is a proposal to the industry for consideration, feedback, and comment.

Summary of Modeling deliverables in Figure 3: Modeling Deliverables:

- Primary Specification Deliverables
 - The provider is responsible for these deliverables
 - It is reasonable to expect them to do this
- Business Conditions Deliverables
 - The provider is responsible for these deliverables
 - Business conditions determine whether the provider supplies these deliverables
- Emerging Usage Deliverables
 - It has not been determined if the provider should provide these items
 - Because of the wide variety of methods for doing this, it is unclear how the provider should do this

The formats of a few of the modeling deliverables have not been defined at this time because no industry consensus has yet emerged to choose from the many existing formats. This group feels that it would be premature to make a decision now, but that there is value in delivering these models. This leaves the decision about the format between the individual provider and the integrator.

1.6 Organization of this document

This document is divided in three sections and seven appendices.

Section 1, Overview, contains an overview of the Analog Mixed-Signal issues and the structure of this document.

Section 2, Specification of Deliverables, contains a detailed description of each modeling deliverable.

Section 3, Design Guidelines, contains design guidelines associated with each line item.

Appendix A, Block-Based Design Methodology, provides a brief tutorial on the block-based design methodology promoted by VSI Alliance.

Appendix B, Digital vs. Analog VSI, discusses similarities and differences between block-based designs for

analog and digital systems.

Appendix C, Current Source Video Converter, contains an example of what is meant by the line items in the context of a virtual component.

Appendix D, VC Delivery Example, provides an example of a typical interaction between the VC provider and the VC integrator.

Appendix E, Future Issues, lists known issues with analog VSI extensions not addressed in this document.

Appendix F, Glossary of Acronyms, provides expansion and a brief explanation of acronyms used in this document.

Appendix G, Bibliography, lists references to documents and publications for additional information.

2. Specification of Deliverables

This section describes all the deliverable items related to an analog/mixed signal virtual component. If a reference is made to another specification, the contents of that document are usually not repeated in this document. If no additional information is required, “no change” will be indicated in that section. If a referenced section requires specific explanation relevant to the analog extensions, only that explanation is provided in this document. If the context of the explanation in any section is unclear, please refer to the corresponding section in the referenced document.

2.1 User Guide

This user guide is similar to a standard data sheet and is meant to be a visual document.

2.1.1 Specification

Specifications for virtual components (VCs) are generally documented and supplied by the VC provider. These specifications describe functional operation, performance, timing requirements, operating modes, and acceptable operational regions of temperature, voltage, etc. The format includes text, charts, tables, block or flow diagrams, and other graphical information. The actual outline and content of the data sheet will be highly dependent upon the VC type and function.

The VC provider needs to describe the socket requirements for testing, such as: test access interface, test vectors, and test methods that are to be applied with appropriate documentation.

The VSIA Deliverables Table (Table 1) summarizes the user’s guide deliverables of the VC being specified.

2.1.1.1 System Description

The system description is in text format, and is written for the user (system designer or VC integrator) to gain an understanding of the functional operation and general applicability of the VC. It contains both implementation and operational information, and can range in complexity from a page or two for simple functions to possibly hundreds of pages for the complex microprocessor.

Programmable functions will need to contain information the user will require to develop needed programs and software. Typical sections are data formats, instructions and commands, control modes, operating modes, test modes, special modes, and features. Reference to appropriate software support tools, such as models, compilers, linkers, and debuggers is also required.

This deliverable is Mandatory (M).

2.1.1.2 Block Diagrams

Block, flow, and/or tree diagrams are generally required for descriptive reference. The diagrams are to provide information on the interaction of key sub-elements of the VC. They should describe:

- Organization
- Structure
- Partitioning
- Data flow
- Critical interactions

In addition to the block diagram, this document should contain a detailed textual description of the blocks and a brief description of the principles of operation of the VC.

This deliverable is Mandatory (M).

2.1.1.3 Register Description

All externally visible states need to be described. All registers important to the understanding, implementation, operation, and programming of the VC need to be described in this section. This description should include:

- Register definition

- Bit-mapping into registers
- Register clocks
- Access requirements for writing or reading these registers

This deliverable is Conditional Mandatory (CM). If registers are present, this deliverable becomes Mandatory (M).

2.1.1.4 Timing Diagrams

The timing diagram is a graphical representation where the clocks, data interfaces, and status are illustrated and valid conditions for the inputs and outputs are identified. For example, on which edge the input is captured and on which edge the output changes. False path designations, timing errors that can be ignored, and setup and hold conditions are also included.

When asynchronous input is used, sufficient information must be provided to avoid problems in verification and test of the VC. Critical information includes:

- Where the asynchronous circuits are used
- Asynchronous circuit structure
- Metsability probability associated with this logic

For the digital I/O, this deliverable is Mandatory (M).

If applicable, it is recommended that a timing diagram be provided for the analog I/Os of the VC. For example, a voltage reference VC would probably not require a timing diagram. For the analog I/O, this deliverable is Recommended (R).

2.1.1.5 Clock Distribution

The VC provider must provide all critical information on clock(s) and clock distribution. For example, VCs must specify interface requirements for the clocks, such as frequency range, duty cycle, rise and fall edges, active edges, relation to other clocks, slew rate, jitter, and clock stop/start conditions.

This deliverable is Conditional Mandatory (CM). If there is a clock, this deliverable becomes Mandatory (M).

2.1.1.6 Bus Interfaces and I/O Configurations

This section describes the interfaces to the VC with the internal functionality assumed to be at the black-box level. This includes:

- Pin list (I/O names, function, and location)
- Bus interfaces and protocols
- Memory and CPU interfaces
- Bus cycle encoding
- Interrupts
- Data rates
- Word formats
- Clocking specifications

In addition, this section should include functional specifications for the input and output ports. This should contain the following information:

- For output specifications:
 - Signal type (current versus voltage, continuous-time versus sampled-data, tri-stated, etc.)
 - Output range
 - Allowable load impedance
- For input specifications:
 - Signal type (current versus voltage, continuous-time versus sampled-data, etc.)
 - Input signal range
 - Input impedance
- Allowable voltages for each pin
- Current required for each pin (static and dynamic)
- Required source impedance characteristics

- A table similar to Table 2 to indicate the pin type

This deliverable is Mandatory (M).

Table 2: Pin Type Information for I/O Configuration

Pin	Internal	External		Test Capabilities	Guidelines
		ESD Protection	Short-Ckt Protection		
x	x			yes	no
y		x	x	yes	yes
z		x		no	no
w		x	x	yes	yes

2.1.1.7 Test Description Summary

The VC provider should describe the socket requirements for the testing to be applied, such as test access interface, test vectors, or test methods. This section enumerates the types of tests, identifies a proposed standards for each, and maps the VC into the test architecture interfaces. The VC provider must document these test methods that are available in the VC. Section 2.5 of this document describes the deliverables that support the testing.

This deliverable is Mandatory (M).

2.1.1.8 Integration Requirements

This section should include:

- Requirements specific to certain VC types as opposed to general requirements. An example might be special noise isolation or power requirements.
- Non-standard files and formats required.
- Explanation of any design condition that could be considered contrary to VSI standard guidelines.

This deliverable is Recommended (R).

2.1.1.9 Schematic Block Diagrams

In addition to block diagrams which often tend to be at a conceptual level, schematic block diagrams are recommended. The intention is for the integrator to use these diagrams to better understand the virtual component. The intent is not to use these for simulation. In general, these diagrams will not contain details that might reveal the IP in the design. The diagrams can be at a mixed-level including detailed schematics only if necessary as an aid for understanding how the VC works. These schematic block diagrams can be provided in any open desktop publishing format.

This deliverable is Recommended (R).

2.1.1.10 Operating Modes

The operating modes for the VC, similar to those listed here, must be provided.

- Power down modes necessary for IDDQ testing
- Functional configurability

This deliverable is Mandatory (M).

2.1.1.11 Bias Supply Management

This document should discuss bias requirements, including the following topics, which are considered relevant:

- Specify whether VC has a built in bias or requires an external bias (magnitude, as voltage or current, tolerance, etc.). Define the bias interface port (BAP), if one is used.
- Specify constraints on drops, matching, etc.
- Voltage reference specification (if used)
 - Voltage level
 - Current drawn
 - Temperature coefficient
 - Source impedance versus frequency
- Bias supply

This specification assumes that an external bias supply will be used for all of the analog VCs used in any design. This bias supply provides current for static power as well any reference voltage.

 - Bias supply requirements (currents)
 - Voltage range allowable

This deliverable is Conditional Mandatory (CM). If there is a bias supply, this deliverable becomes Mandatory (M).

2.1.1.12 Operating Ranges

The operating range for the VC must be documented, including

- Temperature
- Power supply

This deliverable is Mandatory (M).

2.1.1.13 Power Supplies

Power management under all operating modes must be clearly specified, including:

- Definition of power pins
- Constraints on combinable supply pins (dirty, clean supply lines)
- Clean supply (supply that only varies within a certain tolerance)
- Constraints on the amount of deviation tolerated from the norm and the corresponding frequency range
- Maximum inductance
- Substrate noise limits and requirements
- Power supply requirements
 - Voltage level
 - Supply current (peak/mean)
 - Noise requirement
 - Power supply fluctuation requirement
 - Power sequencing requirements (analog versus digital)

This deliverable is Mandatory (M).

2.1.1.14 Electrical Specifications

The electrical specification for the VC should include a list of parameters: such as integral non-linearity (INL), differential non-linearity (DNL), gain, bandwidth with definitions, and calculation methods, including:

- Variations and/or sensitivity over temperature, supply, etc.
- Electrical input and/or output specification
- Typical, minimum and maximum values
- DC and AC specifications
- Test conditions to support specifications

An executable specification may be delivered. The estimator can be used to see if the VC meets the required performance specification. (See Figure 4: Example Estimator Inputs and Outputs.)

In choosing A/MS VCs, a variety of performance specifications have to be simultaneously considered. Because there may be options in the choice of required specifications, a useful model may be the parameterized estimator. Given a set of inputs for performance specifications, the model would return the other specifications. For example, a specification for frequency might return a power estimate. It might also even give a “go” “no go” decision on a set of specifications.

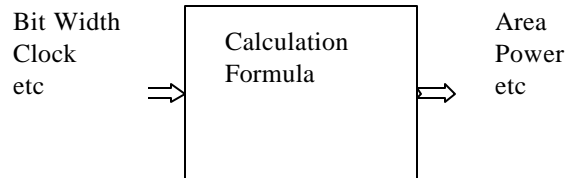


Figure 4: Example Estimator Inputs and Outputs

Potentially, there may be many models of varying levels of detail and many models targeted for different performance specifications. As a result, depending on the question being asked, multiple models may be required. The parameterized estimator tries to tie this together so that a specific VC can be selected.

The estimator can be used to see if the VC meets the required performance specifications. The models may be for different purposes: validating VCs, evaluating VCs performance specifications, system verification, etc.

- Models delivered will be dictated by the type of circuit and customer requirements.
- Models will bound all corners, so no corner models are required.
- Models may be more “active.” They could be “context” monitors where the models act like objects and can evaluate whether or not they are being used correctly; which means that the constraints that are placed for their usage are being validated automatically.
- Because the VC is hard, the analog/mixed signal performance specifications will be process specific.

This deliverable is Mandatory (M).

2.1.1.15 Special Bonding Pad Requirements

A “bonding pad” is defined to include not only the metal geometry where the bond is made, but also all the required support structure (ESD diode protection, digital buffers, etc.). Note that a bonding pad is a VC in itself, so information on the bonding pad (models, physical, etc.) is required in a separate deliverables table. This section should provide the following information:

- Specify which, if any, I/O signals require a special bonding pad.
- Indicate whether multiple connects to the pad are required.

This deliverable is Conditional Mandatory (CM). If special pads are required, this deliverable becomes Mandatory (M).

2.1.2 Claims and Assumptions

Before purchasing, the VC supplier must provide information of features and characteristics of a VC for user evaluation and selection. This will result in claims related to performance, size, number of gates/bits/transistors, power requirements, etc. The VC supplier has the responsibility of substantiating these claims. The supplier is required to define the context to which the claims were evaluated and therefore, validated. This context is referred to as the “reference environment.” The reference environment will consist of the generic technology library, design flow, design tools, options, parameters, and all other information used to implement the VC in this environment. With this reference environment, the user should be able to duplicate the results and verify the VC supplier’s claims.

The VC provider will state the claims for the VC including a minimum of the following:

- Functionality
- Performance (measured or estimated)

- Power usage (measured or estimated)
- Implementation size
- VSI Data Formats table
- Testability
- Test suites and/or test streams

These claims represent the VC supplier's products to the VC integrator. They will represent the supplier's value added, market place differentiation, and will serve the VC integrators in the process of choosing the appropriate VC to meet their needs.

This section should include the key specifications for a typical application. The VC supplier/provider should describe a typical application including: typical, minimum, and maximum values.

This deliverable is Mandatory (M).

2.1.3 Verification of Claims

This section describes the procedures so that the claims made by the VC provider can be verified. Actual measured values can be used when available.

The VC provider must define the reference environment to ensure that it is repeatable. A user would then be able to repeat the provider's claims by duplicating the conditions specified in this reference environment. An audit capability of the provider's claims is provided.

A document identifying compliance with Table 1 deliverables is required from the VC provider. To facilitate such documentation, the VC provider's response is recommended to be in the form of the Deliverables Table, including columns (Comments) for specifying deliverable status.

The verification of claims about the analog VC is critical because of its sensitivity to process. This section may contain the proof that the analog block can work on different processes, listing those on which it has been built. This section provides the following:

- Discussions and results of various test simulations
- Level of checking
- Validation checklist that contains a list of tasks enabling a VC integrator to determine whether a particular task was done.
- List of checks performed (DRC,LVS, LPE and re-simulation) and physical test results, if available.

This deliverable is Mandatory (M).

2.1.4 Version History

The VC provider must supply a version history of the VC describing changes and version releases associated with the VC. This information should clearly identify the current level of release and be coordinated with the claims. This section can also include a usage history.

This deliverable is Mandatory (M).

2.1.5 Known Bugs

A record of bugs, issues, or other problems that are known to exist in a VC must be kept and made available to the VC purchaser/integrator. This section can also include workarounds and plans for fixes.

This deliverable is Mandatory (M).

2.1.6 Application Notes

The application notes should discuss the implementation customization options available to a system designer using the VC. For example, a microprocessor unit (MPU) VC could offer different memory access mechanisms, such as burst access or pipeline access. The VC provider may provide an application note explaining different implementation options to the VC user in designing the memory subsystem unit.

A typical application schematic can be provided. The system design intent will be captured here. Since analog blocks tend to be sensitive to the end application, a range of applications for which this block is applicable can be stated here. The notes cover topics similar to the following:

- It is critical that the purpose of the design is stated, so it is clear what uses may be applicable for the VC.
- Latch-up issues may be discussed here both for protection against latch-up, and to provide operating parameters for the VC to prevent latch-up.
- Restrictions can be placed here. This can be an informal discussion.
- Information that goes with the application of the VC is entered here.
- Issues related to packaging requirements for the VC should be included.
 - Power dissipation
 - Maximum/minimum chip temperature
 - Electrical requirements on package for signals or power
- Shielding strategies can be described here for the VC. However, this is probably not necessary as the blockage file will include this information.

This deliverable is Recommended (R).

See *VSIA Architecture Document 1*, 2.1.6 (Application Notes).

2.2 Process Definition

This section describes the manufacturing process(es) for which the VC was designed.

2.2.1 Process Requirements

This section describes the semiconductor process required in using the VC. This information must be described to a level of detail that will ensure the use of the correct process by the integrator when fabricating the final part. If it is necessary to discuss specific ranges in this process, then this discussion must be included.

This deliverable is Mandatory (M).

2.2.2 Process Tolerances

This section should clearly state the windows of device parameters in which the VC specifications are met. This section is required to help the integrator determine the effect of process tuning on the VC. For example, for a set of allowable process items that can be tuned, the effect upon the VC specifications should be described.

This deliverable is Mandatory (M).

2.2.3 Process Sensitivities

This section should describe the process parameters that affect the functionality, performance or other characteristics of the VC. This information enables an integrator to see how performance specifications vary with process changes. This specification should document the following:

- Performance variations with device parameters inside as well as outside these windows.
- Known sensitivities to processing. For example, the sensitivity of the circuit operation to capacitor oxide thickness, poly resistivity, etc.

This deliverable is Recommended (R).

2.2.4 Process Design Rule Exceptions

Although rare, analog design occasionally violates design rules to achieve unique VCs. If these design rules are intentionally violated, it is mandatory that these design rule exceptions be clearly noted with a detailed explanation.

This deliverable is Conditional Mandatory (CM). If design rules are intentionally violated, this deliverable becomes Mandatory (M).

2.2.5 VC Processing History and Portability

This section should include a list of all the processes into which the VC has been successfully integrated as well as other known processes that are presumed suitable but not yet tested.

This deliverable is Recommended (R).

2.3 System Architecture and Design

The intent of the three models called out in this section, the algorithmic level model, the system evaluation/behavioral model, and the bonded out VC/prototype is to aid the system architecture and system design process.

IMPORTANT: The verification test bench and model validation documentation must be supplied for each deliverable in the system architecture and design and the functional and performance modeling section unless otherwise noted.

Verification test bench for the model should contain the verification setup and the simulation stimulus for the model.

Model validation documentation level of detail may be quite varied. The VC integrator may require documentation to see how the model for a VC was built and may require validation. The VC provider would provide a description of the process here.

2.3.1 Algorithmic Level Model

This model is used by the system architect to investigate necessary trade-offs between different types of VCs in an algorithmic way, if applicable. This is usually a mathematical model describing the functionality of the VC and, when necessary, also models the key behavior (performance specifications) of the VC. For example, a selection between 6-bit or 8-bit A/D converters used in an architecture of a system has to be made to obtain adequate resolution with minimal size. The model could be in any of the high level languages used by other blocks at architecture level, for instance, C++, Java, Verilog, or VHDL. A testbench to verify the algorithm used by the model should be provided.

Currently used formats applied to this deliverable include:

- Simulation Languages (BONes), MAST, Midas, SpretreHDL, VC Hspice, Verilog, VHDL, Verilog-AMS, VHDL-AMS, etc.
- Programming Languages (C, C++, Java)
- Spreadsheets (Excel, etc.)
- Mathematical Packages (Mathematica, MathCAD, Matlab)

Reference the *System Level Design Model Taxonomy*, Version 1.0, Section 4.3 (Algorithm Model).

This deliverable is Recommended (R).

2.3.2 System Evaluation Model / Behavioral Model

This model is needed for system designers to determine the possibility of implementing the system architecture proposed by the system architects. It can be used to help the system architect choose correct VC functions and create specification bounds on the VC.

A system evaluation model or behavioral model describes the functionality and performance of a VC block without providing actual detailed implementation. See Figure 5: System Evaluation Model/Behavioral Model.

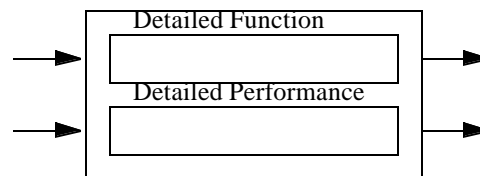


Figure 5: System Evaluation Model/Behavioral Model

Such a model can be parameterized with key options. Because of the close dependency of choice of function with A/MS performance (SNR, linearity, speed of operation, etc.), the behavioral model may need to include key abstractions for the key performance specifications for the VC.

In general the following features define a behavioral model:

- Simple and efficient - The system designer must be able to use the behavioral model to evaluate a number of architectural alternatives in a chip consisting of tens of millions of transistors with several other VCs, each with its own evaluation model. Thus, each evaluation model must be as simple as possible to allow fast simulation speed to determine architectural features quickly.
- Depending on the type of VC, the model may only contain an idealized behavior with a set of bounds on the actual behavior to represent typical degradation from the ideal.

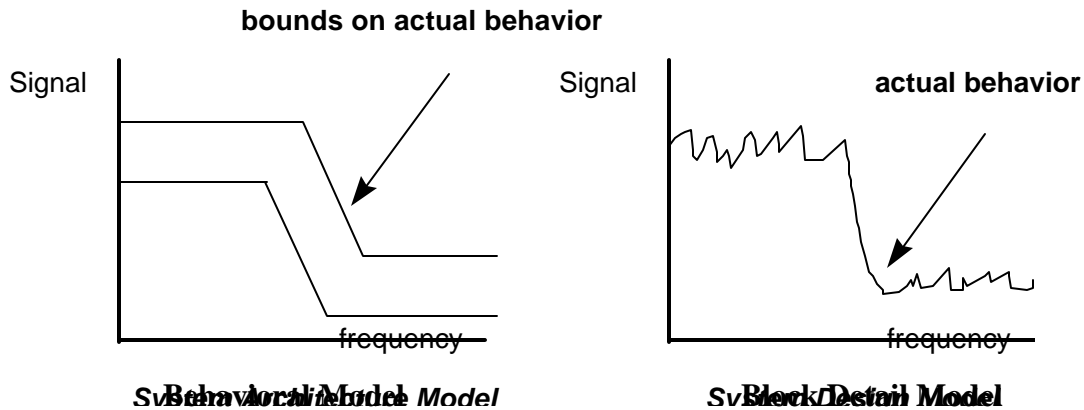


FIGURE 6. EXAMPLE OF BEHAVIORAL MODEL VERSUS BLOCK DETAIL MODEL

The model represents the function and performance and probably not the VC architecture. The model only contains an I/O transfer function for the block. More detailed information from simulation would require other types of models. See Figure 6: Example of Behavioral Model versus Block Detail Model.

A more complex version of this model would also assist in determining the degradation of performance based on external effects on the VC. The model can be in a high level functional description language (c, c++, HDL, etc.). A test bench and test vectors to prove the claimed features and performances should be attached.

Note: More than one model can be provided to measure different performance specifications if necessary.

Currently used formats applied to this deliverable include:

- Simulation Languages (BONes, MAST, Midas, SpretreHDL, VC Hspice, Verilog, VHDL, Verilog-AMS, VHDL-AMS, etc.)
- Programming Languages (C, C++, Java)
- Spreadsheets (Excel, etc.)
- Mathematical Packages (Mathematica, MathCAD, Matlab)

Reference the *System Level Design Model Taxonomy*, Version 1.0, Section 5.2 (Abstract-Behavioral Model). However, analog performances need to be included as well.

This deliverable is Recommended (R).

2.3.3 Bonded Out VC/Prototype

System chips with embedded software frequently require special simulation. Near the end of the design process, to perform integration testing (in which hardware and software run together), a simulation system involving a hardware emulator is evoked. This is done for reasons of functional completeness and execution speed. In order to simulate with a hardware modeler or hardware emulation system, either a high-level model or a bonded out VC is needed for all VCs on the chip. The unavailability of a prototype model as either language based or as a bonded out VC for even one VC can complicate or prevent building a hardware prototype.

The bonded out VC (see Figure 7: Bonded Out VC/Prototype) should be accompanied by measured data.

Typical guidelines for prototype evaluation methods could be:

- The VC integrator may want to verify the Bonded Out VC/Prototypes.
- The VC provider should provide information (schematics, instrumentation) about the physical verification environment.
- The VC provider may also consider delivery of an evaluation board, specification and user's guide for such an evaluation board, and a characterization plan of test circuit prototypes.

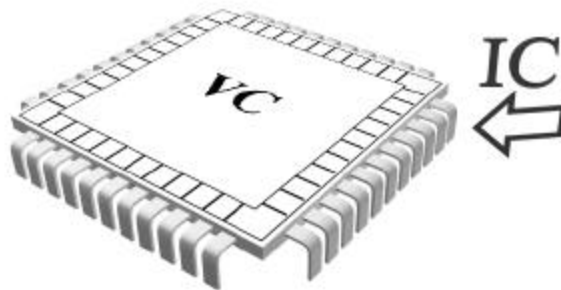


Figure 7. Bonded Out VC/Prototype

This deliverable is Recommended (R).

2.4 Functional and Performance Modeling

The models in this section are intended for a typical chip-level IC (digital) implementation or verification flow. This section represents the models that are used below the boundary between system design and implementation (from RTL to the target library).

2.4.1 Digital Placeholder Model

The intent of the model is to help VC integrators go through a typical digital design environment (HDL, synthesis, floorplanning, timing analysis, test generation, place and route, etc.) which usually is the case for A/MS integration (mostly digital and a small part of A/MS).

This is a very basic model for VC integrators (who usually have a digital background) for integrating an A/MS VC onto a chip with all the other system parts. This model is pin accurate and usually describes minimal functionality and timing information. For example, PLL may only be represented in its bypass mode. More accurate models can be provided as the Functional/Timing Digital Simulation Model (2.4.2) and Block Detail A/MS Mixed-Level Simulation Model (2.4.7). Critical to this model is that it must contain all the VC inputs and outputs. It is not usually necessary to provide a test bench for the model, because it is not intended to be used for verification. The language for the model should be consistent with the language used by other digital parts of the chip.

This deliverable is Recommended (R).

2.4.2 Functional/Timing Digital Simulation Model

The main purpose of the model is to enable VC integrators to tie in functional verification and timing simulation with other parts of the system. This is the model that describes the A/MS VC in a digital simulation language.

This model is pin accurate and describes the functionality and timing behavior (dynamic) of the entire A/MS VC between its input and output pins. This model can be done in many ways. For example, a functional/timing model of a PLL may accurately represent the timing relationship of reference clock input versus generate output clock. This can be modeled by actually representing the structure of the PLL, or it can be modeled as just a delay value based on a simple calculation from some parameters. The activation of the Reset input of a PLL can also be modeled. The model could also:

- Describe behaviors of interest, such as known output states, in a power-down mode.
- Describe how long it would take for the PLL to generate the output clock.
- Be in any high level digital HDL.

The model is behavioral and is not meant to be synthesizable. A testbench should be delivered along with the model.

The model does not provide any synthesizability to the VC, rather a high level functional and timing description. Instructions must specify how to do simulation with a test bench and required simulators.

Reference the *System Level Design Model Taxonomy*, Version 1.0, Section 6.1 (Detailed-Behavioral Model). Note that only an approximation of the analog behavior is included in this model.

This deliverable is Recommended (R).

2.4.3 Digital Timing Model for Static Verification

The purpose of this model is to allow VC integrators to go through their standard digital flow with respect to clock design and timing verification.

The model contains static timing information of the digital portion of the A/MS VC and can be used in cases where static timing analysis is used in conjunction with all of the other VCs for timing analysis. Although the static timing information is not meaningful for the VC analog signals, this model has to contain “pseudo-static timing” so that the VC can be integrated. For example, a typical digital sign-off procedure might require the results of the static timing analysis. Therefore, by treating analog signals as digital and modeling them in digital fashion, the design environment can accept the VC. The digital signals of the VC, however, have to be modeled precisely like all other digital circuits. For example, in the circuit below, the timing information between the digital control and digital data should be modeled in the same way digital timing is modeled. However, the timing information between digital control and analog out may have to be generated for analog circuit simulator or entered based on an estimate. Since static timing verification is only relevant to digital signals, an estimate from digital to analog is only there as a placeholder for sign-off and probably will not be used. (See Figure 8: Example Timing Arcs for the Digital Timing Model for Static Verification.)

Note: A test bench is not required for this model.

See *Soft and Hard VC Structural, Performance and Physical Model Specification 1*, Version 2.0 (I/V 1 2.0 Sections 2.2.1 (Basic Delay Model) and 2.2.2 (Timing Analysis Model). The timing analysis model is a superset of the basic timing model containing additional timing characteristics. The model for A/MS blocks should contain sufficient information for static verification. However, because of the relative simplicity of the digital interface for the A/MS blocks, many of the attributes required for these models are not applicable.

Currently used formats applied to this deliverable include lib/Stamp, ALF/DCL/OLA.

This deliverable is designated Recommended (R) rather than Mandatory (M). Typically, the number of pins for the digital sections of AMS VCs is relatively small. Thus, the digital case can usually be handled by a method not fully automated.

For more complex digital sections with many pins, a digital static timing model may be required to provide an automated method for chip level routing. However, since such digital usage is not yet a well established industry practice, this deliverable remains Recommended (R) for AMS blocks.

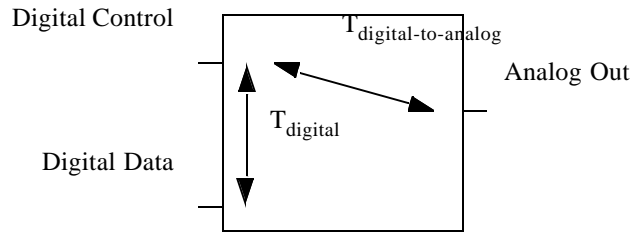


Figure 8: Example Timing Arcs for the Digital Timing Model for Static Verification

2.4.4 Bus Functional Model

The purpose of this model is to allow VC integrators to go through their standard digital flow with respect to bus functional verification.

This model describes the bus functions of the digital interface for the A/MS VC. The purpose of the model is to provide a higher level description of A/MS VC bus functions, so that an integrator can use it to do bus functional simulation with other VCs on a chip. For example, a PLL might have a setup register. The bus functional model would be used in the same way as a digital VC with a setup register. Analog inputs and outputs are not considered as buses. The model is in the same language as that used for the digital blocks. A test bench with examples should be provided to integrators.

The intent is to separate verification of the internals of the VC and the interfaces of the VC. This model focuses on the functional interface of the VC. For example, if four VCs are required to be integrated on a chip, the methodology may be as follows:

- Verify each of the blocks A, B, C and D independently (see Figure 9: Example VCs in SOC).
- Verify only the interconnects between the blocks to get the full coverage.
- Verify further by combining relevant or interconnected blocks.
- Full chip verification can be done when applicable (and necessary), but it is assumed that the majority of the chip will not have any interaction with the analog blocks.

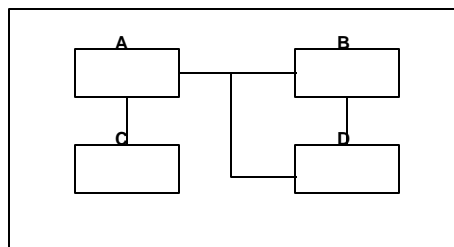


Figure 9: Example VCs in SOC

The description language for the bus functional model will be the same language as that used for the digital blocks, because the bus functional models will be used to test that *all* the blocks work together.

Currently used formats applied to this deliverable include Programming Languages, Verilog, VHDL.

Reference the *System Level Design Taxonomy*, Version 1.0, Section 3.2.2 (Interface Model).

This deliverable is Recommended (R).

2.4.5 Peripheral Interconnect Model

This model is only for the digital interface of the A/MS VC. The model is used to accurately calculate the interconnect delays and output cell delays associated with the VC.

The peripheral interconnect model represents the interface interconnect network shell around the internal VC delay model. It models the wire stubs from the output buffer to the VC physical boundary in terms of Rs and Cs. The same is true for the inputs. This model is specified by a fully distributed RC tree representation.

Note: A test bench is not required for this model.

See *Soft and Hard VC Structural, Performance and Physical Model Specification 1*, Version 2.0 (I/V 1 2.0) Section 2.2.4 (Peripheral Interconnect Model).

This deliverable is Conditional Mandatory (CM).

If there is a measurable level of interconnection between the I/O ports and the internal gates of the VC, this deliverable becomes Mandatory (M).

2.4.6 Electrical Port Models

A circuit level description of the electrical characteristics of the A/MS VC interface is recommended. An A/MS VC interface, however, is usually composed of digital and analog ports. The deliverables which have been separated are covered in the following sections:

2.4.6.1 Digital Electrical Port Model (Device Level Interface Netlist)

See *Soft and Hard VC Structural, Performance and Physical Model Specification 1*, Version 2.0 (I/V 1 2.0) Section 2.2.5 (Circuit Level Interface Model)

Reference the *System Level Design Model Taxonomy*, Version 1.0, Section 6.6 (Circuit Level Model). This would be for the digital interfaces.

This deliverable is Recommended (R).

2.4.6.2 Analog Electrical Port Model

The purpose of the model is for system integrators to validate the system interface. This is used to provide the interface features of a VC.

This model describes the electrical behavior of the analog interfaces. Typically, input and output buffer characteristics are described in Hspice-level granularity. System integrators can use this model to validate the electrical characteristics of the analog ports. This differs somewhat from the digital representation. The Analog Electrical Port model combines the information in the peripheral interconnect model (2.4.5 above, I/V 2 2.2.4) and the digital electrical port model (2.4.6.1 above, I/V 2, 2.2.5). Thus this model has the input devices, output drivers, and resistors and capacitors associated with the wires within the VC. A test bench should be provided.

Reference the *System Level Design Model Taxonomy*, Version 1.0, Section 6.6 (Circuit Level Model). This would be for the analog interfaces.

This deliverable is Recommended (R).

2.4.7 Block Detail A/MS Mixed-Level Simulation Model

This model allows the integrator to simulate at the VC level quickly. It takes advantage of behavioral modeling techniques to model non-critical blocks. Only critical elements are modeled in detail. One use of this model is to assist integration engineers with VC qualification.

The block detail A/MS mixed-level simulation model is a functional model composed of block sub-models for detailed functions. These block sub-models typically are in high-level behavioral description, and only the critical functions use gate or transistor-level structural modeling techniques. The ports of the VC are modeled accurately. An example for a PLL VC is as follows. The charge pump and the filter might use circuit-level accurate models. The phase detector might be done at a high-level with either a digital high-level description language or an analog high-level description language. The VCO might be done at a high-level with an analog high-level description language.

By taking advantage of the behavioral level description, this model enables a VC integrator to do mixed-level, mixed-mode simulations faster than would be required at a detailed circuit level. Therefore, this model could elaborate the detailed functionality of the VC behaviorally and/or structurally if the mixed-level of subblocks is used. A test bench and requirements for simulators used should be included with the original model delivery.

Currently used formats applied to this deliverable include Verilog-AMS, VHDL-AMS.

Reference the *System Level Design Model Taxonomy*, Version 1.0, Section 3.2.3 (Mixed-Level Model).

This deliverable is Recommended (R).

2.4.8 Detailed Transistor/Gate Level Schematics

The main purpose of the schematic is for understanding the VC (functionality and performance).

This schematic contains a full graphical description of the circuit at transistor/gate (intermix gates and transistors) level including relevant parametric values of the devices. Typically, parasitics of the circuit are not included, but critical anticipated ones may be included. The schematic is not meant to replace the netlist in 2.6.7 but to help the integrator obtain a detailed understanding of the implementation of the circuit functionality (such as what kind of temperature compensation is used for the circuit). The format can be hard copy or electronic copy. Test bench and model validation are not applicable here.

Currently used formats applied to this deliverable include EDA Proprietary Database/Formats, EDIF 2.0, EDIF 2.0 document.

This deliverable is Conditional Recommended (CR). If the VC provider agrees to release this deliverable, it is Recommended (R). They may be IP Protection issues requiring discussion between the VC provider and the VC integrator.

2.4.9 Circuit Level Simulation Netlist

The purpose of this netlist is primarily for simulation not LVS (see Section 2.6.7). The netlist should be commented so that it is more designer intelligible (possibly hierarchical). With the application of stimulus, the netlist should also serve the purpose of specification validation. A netlist in escrow may also serve as insurance for the VC integrator.

The simulation netlist uses basic IC devices (resisters, capacitors, transistors, etc.) with optional inclusion of parasitics for verification. The recommended format for the netlist is VC Hspice. Application notes including all relevant simulation instructions, verification testbenches, required models, model validation methods, detailed settings, suggested simulators, and simulation results should be provided.

Reference the *System Level Design Model Taxonomy*, Version 1.0, Section 6.6 (Circuit Level Model). This would be at transistor level.

This deliverable is Conditional Recommended (CR). If the VC provider agrees to release this deliverable, it is Recommended (R). They may be IP Protection issues requiring discussion between the VC provider and the VC integrator.

2.5 Test Support

This section describes the deliverables to support manufacturing test for the VC.

2.5.1 Signal Requirements

This section lists the signal requirements and provides additional information about these signal requirements.

- Digital vectors required to put the VC in test mode or to set up for a particular condition should be applied by a scan chain; the vectors may be supplied in STIL (IEEE 1450) format.
- Where possible, access for test signals, including built-in self-test (BIST), to the VC should be through an IEEE 1149.1-type scan path for digital, and an IEEE 1149.4-type path for analog, unless the access points are intended to be padded-out.
- Digital signals (those which create an analog signal in the VC) should be supplied in a separate file. The file should contain a header which specifies, at a minimum, the number of bits which constitute a word and whether the file is organized as MSB or LSB first. If the sampling rate is not derived from the clock accompanying the digital vectors, it should be specified also.

- Analog signals should be specified by parameters which would allow them to be created completely, if they are being sourced, or by specifying which parameters need to be measured. Examples of such parameters are: frequency, amplitude, phase, and D.C. component. If an industry-standard method of describing analog signals for test is adopted (as STIL does for digital vectors), then this may be used.
- Any special requirements for the test signals should be specified, such as minimum bandwidth paths, load conditions etc.
- The accuracy required of an instrument to faithfully produce or measure any analog signal should be specified.

This deliverable is Mandatory (M).

2.5.2 Test Requirements

This section lists the test requirements and provides additional information about these test requirements.

- Tests must be supplied that provide a manufacturing test of functionality and conformance to specification. Any published specification which is not guaranteed by the suite of tests included must be labeled as not covered.
- All test signals must be specified as outlined above. Use of specific instruments in a test setup is not sufficient, as the integrator may not have access to the instrument or it may be unsuitable for manufacturing test.
- Any tests that require circuitry external to the VC should be shown on a schematic. Only circuitry that can be applied to external padded-out pins, or can satisfactorily be connected through the two-wire IEEE 1149.4-type bus, is allowed.
- Where possible, estimates of the test time for each test should be provided (assuming the target tester does not add any overhead). Device settling times should be separately identified. This will allow the integrator to estimate his final manufacturing test time, or to skip tests which he believes would be unacceptably long in production. Only the integrator can make this determination, since he is responsible for the quality of the final product. If a particular manufacturing tester is assumed for estimating test times, then the model must be specified.

This deliverable is Mandatory (M).

2.6 Physical Block Implementation

The deliverables called out in this section are directly related to the physical integration of the VC.

2.6.1 Detailed Physical Block Description

The detailed physical block description is the physical implementation of the VC at the polygon level.

Currently used formats applied to this deliverable include GDSII-Stream, LEF/DEF, SPICE.

See *Soft and Hard VC Structural, Performance and Physical Modeling Specification 1*, Version 2.0 (I/V 1 2.0), Section 2.3.1 (Detailed Physical Block Description).

This deliverable is Mandatory (M).

2.6.2 Pin List/Pin Placement

See Section 2.6.4, Footprint.

Currently used formats applied to this deliverable include LEF/DEF.

See *Soft and Hard VC Structural, Performance and Physical Modeling Specification 1*, Version 2.0 (I/V 1 2.0), Section 2.3.2 (Pin List/Pin Placement).

This deliverable is Mandatory (M).

2.6.3 Routing Obstructions

See Section 2.6.4, Footprint.

Currently used formats applied to this deliverable include LEF/DEF.

See *Soft and Hard VC Structural, Performance and Physical Modeling Specification 1*, Version 2.0 (I/V 1 2.0), Section 2.3.3 (Routing Obstructions).

This deliverable is Mandatory (M).

2.6.4 Footprint

The VC footprint data must be provided in VC LEF format to be compatible with digital VC footprint data. The VC LEF format document should contain

- Pin list
- Pin location
- Block size
- Routing constraints
- Annotated stream with text markers identifying name of each pin and polygonal boundary.

Currently used formats applied to this deliverable include LEF.

See *Soft and Hard VC Structural, Performance and Physical Modeling Specification 1*, Version 2.0 (I/V 1 2.0), Section 2.3.4 (Footprint).

This deliverable is Mandatory (M).

2.6.5 Power and Ground

Analog block power supplies must have a power supply name that is different than digital supplies e.g. VDDA, VSSA, GNDA.

Currently used formats applied to this deliverable include LEF/DEF, ASCII.

See *Soft and Hard VC Structural, Performance and Physical Modeling Specification 1*, Version 2.0 (I/V 1 2.0), Section 2.3.5 (Power and Ground).

This deliverable is Mandatory (M).

2.6.6 Layer Mapping Table

The layer mapping table document describes the GDSII-Stream Level and data-types for each design layer in the database.

2.6.7 Physical Netlist

The primary purpose of the physical netlist is for LVS (layout versus schematic).

Currently used formats applied to this deliverable include SPICE, Verilog-AMS. (An emerging format is VHDL-AMS.)

See *Soft and Hard VC Structural, Performance and Physical Modeling Specification 1*, Version 2.0 (I/V 1 2.0), Section 2.1.2 (Cell Level and Circuit Level Netlist).

This deliverable is Conditional Mandatory (CM). This deliverable becomes Mandatory (M) if the VC integrator requires a layout versus schematic.

2.6.8 General Physical Rules

2.6.8.1 Physical Isolation Specification

Additional required well protection outside of VC, if required, should be described here. If additional well protection is required, its type must be documented.

This deliverable is Mandatory (M).

2.6.9 Placement Specifications

2.6.9.1 Placement Constraints

All placement constraints related to the analog VC must be documented, such as:

- Floorplanning constraints (for example, the types of adjacent blocks that are allowed or not allowed).
- Required symmetry with respect to heat sources and stress constraints (for example, the block cannot go in a particular corner of the chip).

This deliverable is Mandatory (M).

2.6.9.2 Proximity Effects

All proximity effects must be documented, such as :

- Heat Dissipation
- Noise consideration

This deliverable is Mandatory (M).

2.6.10 Interconnect Specifications

2.6.10.1 Special Hookup Guidelines

Any special hookup guidelines should be placed here. For example, special requirements on I/O lines can be placed here.

This deliverable is Mandatory (M).

2.6.10.2 Routing Constraints

The routing constraints for an analog VC should be provided with the following information:

- Geometry constraints
- Critical signal routing constraints
- Impedance constraints
- Required isolation from digital nets (may include minimum spacing allowed to closest digital and analog blocks, physical size, and routing guidelines)
- Constraints for high frequency signal lines
 - EM, inductive effects
 - Length of wires
 - Differential
 - Shielded routing or strip line routing
- Voltage/Current Dependencies (ECL/CML logic)

This deliverable is Mandatory (M).

2.6.10.3 Special Pin Requirements

- Pad routing, loading constraints, etc.

This deliverable is Mandatory (M).

2.6.10.4 Additional Power, Ground and Substrate Interconnect Constraints

- Constraints on power and ground
- Separation of power pins
- Number and type of rings required

This deliverable is Mandatory (M).

2.6.11 Substrate Sensitivity/Constraints

- Substrate noise requirements

3. Design Guidelines

This section contains design guidelines for some of the line items listed in Section 2. At present, all the guidelines described here are considered optional and are proposed for discussion. In the future, the deliverables table might have a rating associated with them (mandatory, conditionally mandatory, etc.). As more suggestions come in, the guidelines listed here may change and new guidelines may be added.

The section number in parentheses matches the entry in Section 2 for easy cross-referencing. If a topic does not have specific guidelines, there will not be an entry in this section.

3.1 User Guide

Operating Modes (2.1.1.10)

- Sleep mode - Analog VC can incorporate a “sleep” mode under external control.
 - Total supply current in “sleep” mode that is compatible with digital IDDQ testing.
 - The actual current level for “sleep” mode will be specified.
 - VC Provider to specify the time required to become operational after sleep mode is turned off and time required to reach specified stand-by level when sleep mode is turned on.

3.2 Test

Test Methods (2.5.2)

General guidelines to test analog or mixed signal VCs:

- There are five main forms of mixed signal circuits:
 - Digital-in/digital-out (i.e. PLL),
 - Digital-in/analog-out (i.e. D/A)
 - Analog-in/digital-out (i.e. A/D, comparator)
 - Analog-in/analog-out (i.e. opamps)
 - More complex I/Os, digital-in, analog-in/analog-out (i.e. switched cap. circuits).
- Analog feedback paths should be kept internal to the VC circuit blocks.
- If IDDQ testing is required, provisions should be made such that the analog circuitry will not interfere with the test. For example, analog blocks should have a power down mode where no D.C. current flows through the analog logic and all digital outputs of analog logic blocks go to valid digital states (high Z outputs are not allowed). The mechanism for achieving this state should be well documented.
- Mixed signal circuits
 - For digital-in or digital-out signals, logic in the analog VCs should follow the requirements and recommendations for testing as described in the digital VC, i.e. scan, BIST or other approaches for digital test. Appropriate test control, data in and data out pins must be identified and provided. A set of test vectors in a tester-independent format such as STIL, and a description of tests performed on the VC logic, should be documented. PLLs would be a special case. A bypass of the PLL clock output should be provided to make low speed (e.g. IDDQ tests) testing possible. If jitter tests or other checking of the PLL operating in normal mode is required, the clock output can be sent directly or via a mux to an output of the IC.
 - For analog-in or analog-out signals, paths to the signals should be routed to the test bus unless it would compromise the desired performance of the VC, or if the signal is primarily intended for connection to an IC pad. In the latter case, if observability is required, providing access to such signals for test is the responsibility of the VC integrator.
 - For signals connected to IC pads (primary), digital signals connected to IC pads may be tested using methods described in the recommendations for testing a digital VC. Analog signals coming from the IC pad would require functional testing to assure proper operation (type 2 circuits). The correct digital output for the corresponding analog input must be provided. Analog signals going to an IC

pad would also require functional testing to assure proper operation (type 3 circuits). The digital inputs for the analog output must be provided.

- o Internal digital inputs and outputs (signals not connected to IC I/Os) should follow the requirements and recommendations for testing a digital VC with the addition of the tests described in Section 2. (See Figure 10: Test Bus.)

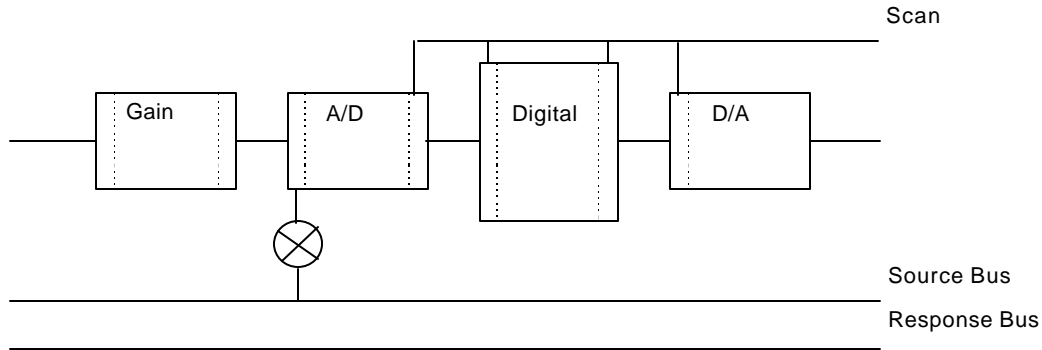


Figure 10: Test Bus

Explanation of the “Test Bus” circuit:

The VC blocks

- Each of the blocks, Gain, A/D, Digital, D/A, is assumed to be a VC acquired by the system integrator.
- The A/D and D/A blocks provide test access for their digital ports in the form of serial streams that can be tied into an internal scan chain. No analog test access for the D/A is provided by the VC supplier, who has stated in his documentation that the analog port is suitable for connecting directly to an outside pad. Any access required must be provided by the integrator.
- The gain block has test access at both its input and output.
- The impedance of analog test access points must be specified so the integrator can determine the best means of connecting them to a test bus.

The Test Bus

- A two wire test bus is provided similar to that specified in IEEE 1149.4.
- The intent of the bus is modified to provide for internal access rather than just testing out to the pins.
- Internal logic (not shown) is assumed to be provided by the integrator such that only one analog signal can be connected to either the response or stimulus bus simultaneously.
- Providing sufficient bandwidth in the design of the bus for probing test access points on the chip is the responsibility of the integrator.
- Buffers may be required between the analog test points and the bus if the impedance of the test point is too high.
- The input of the A/D is connected to the source wire of the test bus by a FET switch, as the integrator believes that testing the A/D separately is a requirement.

3.3 Physical Block Implementation

Layer mapping table (Section 2.6.6)

Both hardcopy text and ASCII file can be provided as part of the documentation along with GDSII data.

Pin List/Pin Placement (Section 2.6.2)

I/O pins will exist at the outside edge of the VC block.

Footprint (Section 2.6.4)

VC LEF format file should contain abstract view of block.

Power and Ground (Section 2.6.5)

Analog supplies connected on chip should be tied in a star pattern at the supply pad.
Clean and dirty supplies should be kept separate and outside the package.

Physical Netlist (Section 2.6.7)

The physical netlist of the VC may be required to validate the VC and connect it to other elements.

General Physical Rules (Section 2.6.8)

Well Protection

Sea walled blocks - Analog VCs can be individually sea walled to minimize the effect of digital noise and circuit interaction. For example, the sea wall should be strapped with metal around the whole circuit except at the I/O points, but the sea wall in silicon should not be broken at any point.

For an *n-well* process, the structure should contain a complete ring of $p+$ enclosed by a ring of $n+/nwell$ enclosed by a ring of $p+$. The inside and middle ring should be tied to the analog supply and the outside ring to the digital supply. For mixed-signal circuits, the analog portions should be contained in a full sea wall structure with the digital portions walled with a $p+$ ring (see Figure 11: Well Protection Example).

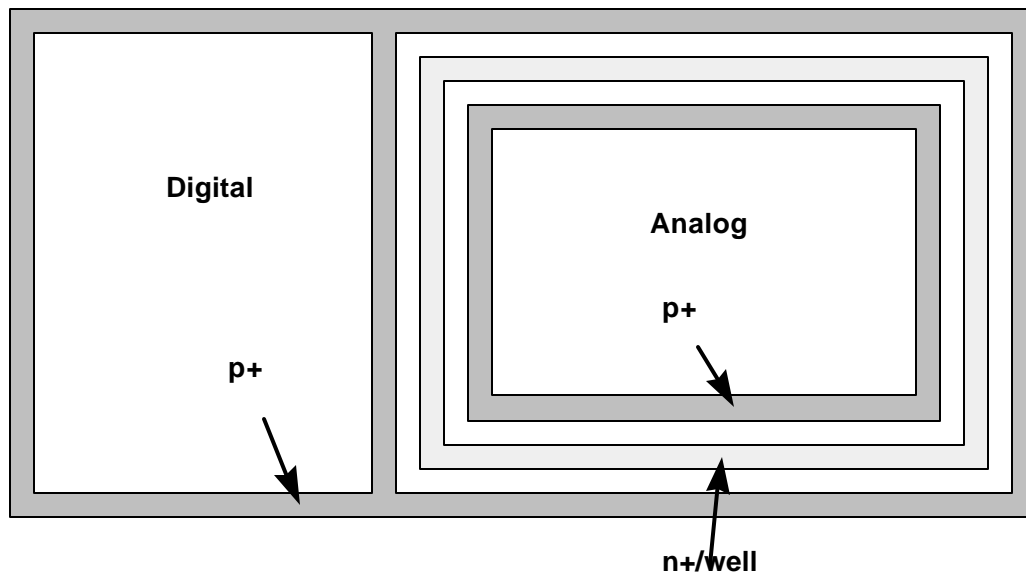


Figure 11: Well Protection Example

Sea walls for each VC should be maintained separately. This will provide the maximum isolation between digital noise and crosstalk from other VCs.

Placement Constraints (Section 2.6.9.1)

The following guidelines for placement constraints are suggested:

- Grids internal to the VC should be as large as possible
- Grids for I/O pins should conform to the current VSIA specification
- Analog VCs should be placed together and on the chip edge
- For maximum isolation, analog blocks may be restricted to a completely isolated corner of the chip, where even digital pads are not allowed, and sea well should completely isolate that region of the chip.

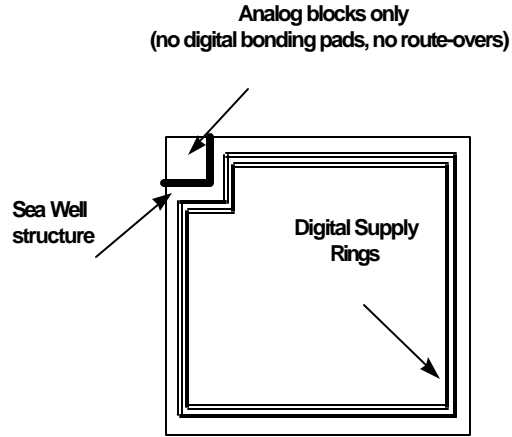


Figure 12: A/MS Block Isolation

- A more moderate approach may be to just split the power ring, but allow interconnect routing within the channels between the analog VC and the analog bonding pads.

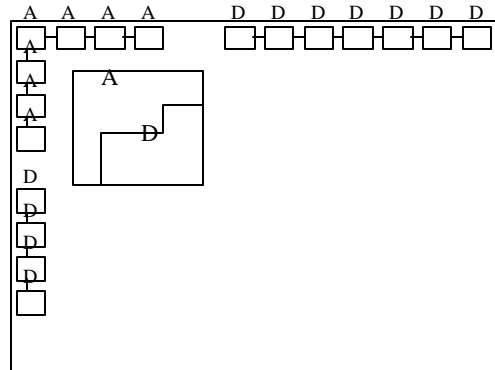


Figure 13: A/MS Bond Pad Isolation

Routing Constraints (Section 2.6.10.2)

A first pass conservative rule is that no routes should be made over analog components.

A. Block-Based Design Methodology

A.1 Introduction

Block-based, core based, or system-level macro (SLM)-based design is a new design methodology created from the *discontinuity* of shrinking process sizes, e.g. 0.25 μm and 0.18 μm processes, where entire systems are integrated on a single chip using complex functional building blocks. The shrinking process size allows for an increasing number of devices to be integrated onto a single chip. The cutting edge of a design is its complexity and time-to-market (TTM), not the performance.

The development of the digital Virtual Socket Interface (VSI) is the result of trying to adapt to this reality. The IC complexity space has grown to a size that is increasing difficult to manage. VSI simplifies the management of this complexity problem by partitioning the IC design space into two worlds. These two worlds are Virtual Component (VC) integrators and VC authors with VSI. This is analogous to the split between the board world and the IC world where the interface consists of data sheets, packaging standards, bus standards, voltage-level standards, etc. This split gives the board designer the ability to abstract the components into manageable pieces for their design. This abstraction also addresses TTM constraints by allowing for the re-use of VCs, analogous to the re-use of ICs. Since VCs now become designed entities of their own with a standard delivery mechanism, the same VC can now be re-used in many VC integrations, thus reducing overall design times.

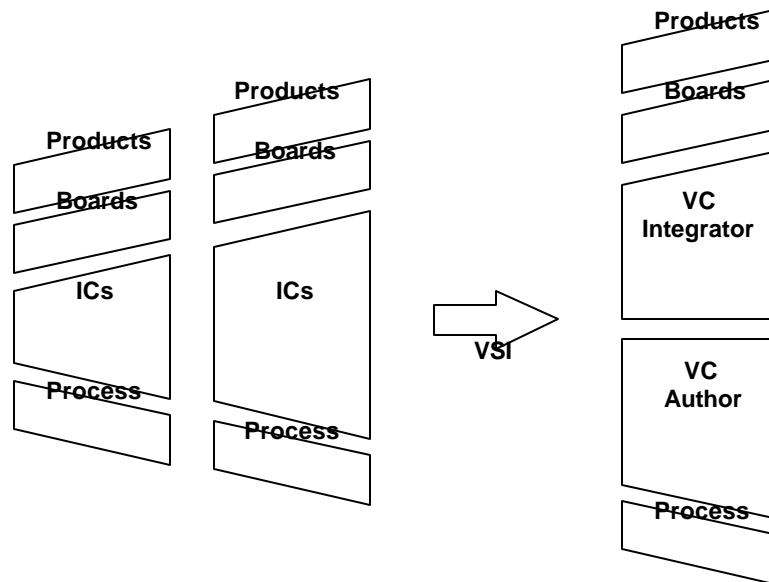


FIGURE 17. FRAGMENTATION OF IC DESIGN

A.2 Market Scenario for Block-Based Design

This section discusses a complementary argument for block-based-design processes. Today, we have systems on boards, made up of “real components” or ICs. System designers select the best Intellectual Property (IP) from different vendors. These VCs can be micro-processors, micro-controllers, DSPs, memory, data converters, etc. Few companies can design enough VCs to build a system entirely of their own VCs. However, with 0.25mm and 0.18mm processes, these systems of today will be system-chips of tomorrow with all of the VCs integrated into one chip. With many of these system applications being in the consumer space, time-to-market and complexity control will be the main design constraints. If it is true that a single company cannot develop enough ICs for these systems today, then reliance on third party VC sources will probably remain the same in the future, and one or more parts of various chips will have to be exchanged. In any case, re-use of VC blocks will be absolutely essential whether it is done internally across a large company or by VC acquisition from third party VC sources. System chip design will have to focus on not only designing the blocks, but also the interfaces between the blocks. On-chip busses, protocols, etc. between the blocks will become critical to the design.

The VSIA vision is to split block authoring and block integration into two different worlds so that the problem can be separated. The separation also allows for the re-use of VC blocks. The system integrator is just left with the problem of assembling the blocks together to create the new system-chips of the future.

A.3 Necessity for Analog Virtual Components

In many market segments (e.g. telecom and multimedia), the need to integrate analog components is high because of the need to interface to the *real* world. The level of integration of analog components such as D/As, A/Ds, and PLLs on large digital chips has been continually rising due to cost, power, and size requirements. See [3] in Appendix G.

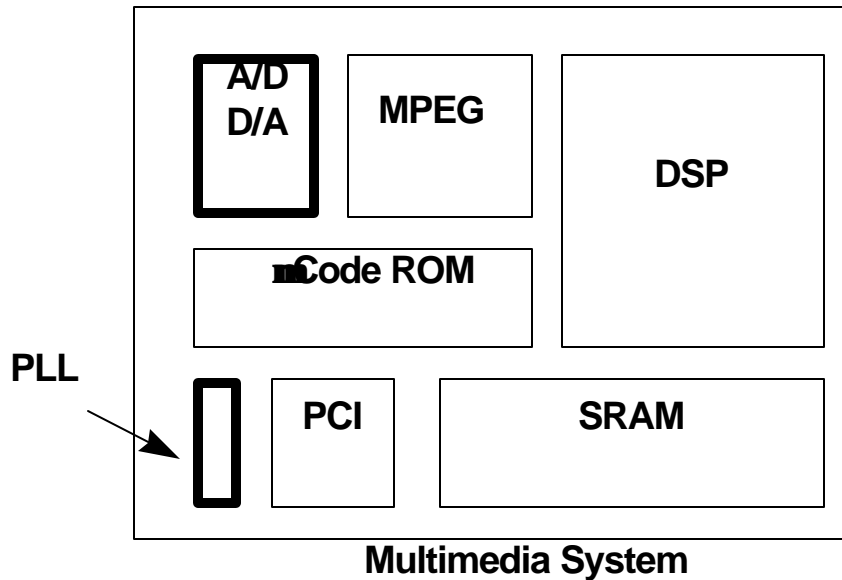


Figure 15. Example SOC with A/Ds VCs

A.4 Need for Analog/Mixed-Signal VSI

The VC author and the VC integrator need an interchange standard to facilitate the process of integrating analog/mixed-signal components into predominantly digital designs. It is critical that only one standard exists, and that it is open so everyone can use it. In this way, integrators and authors will not have to expend extra energy developing or integrating using multiple *ad hoc* or existing standards.

Another driving force for the extension of the VSIA standard is that the current VSIA standard addresses digital VCs but leaves out analog and mixed-signal VCs. Since a block-based methodology using VSI will be well established, it is important to extend the standard based on this methodology to provide the integration of analog and mixed-signal VCs with digital VCs.

The practice of outsourcing analog/mixed-signal blocks exists today. However, the process of delivery of the resultant intellectual property is very tedious for the following reasons:

- Standards do not exist.
- The formats used to deliver the VC data vary considerably depending on the customer and the VC provider.
- Usually, more data than required is shipped because there is no standard for what information must be shipped.

As a result, entire databases are often shipped by VC authors who must prepare the data with

- Different tool suites
- Different library environments within those tool suites
- A lot of time and effort

The goal of the VSI Alliance is to eliminate these problems and make it easier for both the VC integrator and the VC provider. Both the VC integrator and the VC provider can tailor their design methodology to an agreed upon standard and greatly reduce the time spent discussing what needs to be shipped.

An analog/mixed-signal VSI extension will facilitate the growth of the IC market space. With the increase in complexity, it is likely that no one system integration team will be able to provide all the VCs necessary. Third party VCs will be increasingly in demand. An analog/mixed-signal VSI extension would not only allow for more systems-on-a-chip to be created, because there will be access to a wider variety of analog/mixed-signal VCs, but will increase the analog VC provider market, because an analog VSI facilitates VC use. Where VC providers and VC integrators exist in one company today, this extension can also serve as an internal standard for VC exchange.

B. Digital vs. Analog VSI

This appendix provides information about some of the important similarities and differences between the VSIA standards for digital and analog/mixed-signal VCs.

B.1 Similarities

B.1.1 VSIA Standard

- The VSIA standard provides a clear demarcation between the VC provider and the VC integrator.
- The primary VSIA deliverables are the same. Both digital and analog/mixed signal VCs have user guides, system architecture sections, system design sections, test requirements, and physical block implementation sections.
- Analog/mixed-signal blocks contain digital circuitry which should be compliant with the current VSI.

B.2 Differences

B.2.1 VSIA Standard

- An additional section, process definition, is required for the VSIA deliverables.
- Many of the current VSIA deliverables sections are extended to cover critical effects for analog/mixed-signal components and signals.
- Additional considerations are necessary because analog signals are continuous, not discrete.
- Unintended interaction between blocks through power rails or substrate creates design concern for analog circuits.
- A digital VSI is not necessarily sufficient for the digital circuitry inside a mixed-signal block. Situations where digital extensions are required are documented.

B.2.2 Abstraction Level

Because of the additional technology and application specific considerations for design and integration, analog functions cannot be abstracted like digital functions.

B.2.3 Soft, Firm, and Hard Blocks

- This first pass analog standard only considers process specific hard blocks.
- Typically, an analog design is not as portable as a digital design. Therefore, the initial goal is not portability, but the ability to integrate (e.g. PLL with micro-controller chip, A/D with DSP chip). A future goal would be portability.

B.2.4 Input/Output

- Analog interfaces are more complex than digital interfaces because of signal level issues and tighter constraints on impedance levels.
- Different types of interfaces exist in analog/mixed-signal VCs
 - Continuous voltage in, digital bus signal out
 - Digital bus signal in, continuous voltage out
 - Continuous voltage in, continuous voltage out
 - Frequency in/digital signal out, etc.

B.2.5 Testing

- Acceptance of manufactured analog components follows different criteria than digital components.

B.2.6 Process Dependencies

- Analog designs often require components not standard to all processes, such as resistors and capacitors.
- Processes which give similar performance for digital circuits may not do the same for analog circuits since analog circuits are concerned with speed, noise and various other process dependent characteristics.
- Typically, given the same amount of effort, the range of processes to which an analog design can be ported is smaller than digital.

B.2.7 Environment Dependencies

- The performance of an analog component can be highly sensitive to environmental conditions such as voltage supply, swings and temperature.
- The performance of an analog component is critically dependent upon the lithography tolerances (matching).
- Typically, given the same amount of environmental tolerances, analog circuits will be more susceptible to failure than the digital circuits.

B.2.8 Design Guidelines/Rules

- For analog circuits, typical design guidelines are used by the VC developer to control what happens throughout the entire IC. Those guidelines become rules for the VC integrator because the integrator may not have the expertise to determine whether a guideline is necessary. Therefore, a rule can be a conservative set of guidelines where absolute performance or area savings would be sacrificed to ensure that an analog VC can be integrated per specification.
- An implication of the above is that the standard should clearly state whether or not a guideline is mandatory, conditionally mandatory, or optional, similar to the tables for deliverables.

C. Current Source Video Converter

An example VC, a Current Source Video Converter (CSVC), is presented here to illustrate the VSIA deliverables listed by the line items in Section 2. It is neither meant to provide strict guidelines about how one might deliver a D/A converter, nor is it meant to validate this extension document. In some cases, the specified deliverables might seem a bit extreme, but this was deemed necessary since not all the line items are completely applicable to this circuit.

This example is currently a work in progress. It will be developed and validated in the future with the intent of being a complete specification. At this time it is not a complete specification and should only be used as a general guideline.

During the development of this document, this example helped clarify what was meant by line items in Table 1, the VSIA deliverables table. The deliverables for each line item are described in the following sections.

C.1 User Guide

C.1.1 Specification

C.1.1.1 System Description

This 8-bit Current Source Output Digital-to-Analog Converter is suitable for video driver applications. Specifically, the current level ranges have been designed for standard PC and workstation monitor input at the red, green, and blue (RGB) terminals. See Figure 16: Video D/A System Description Pictorial

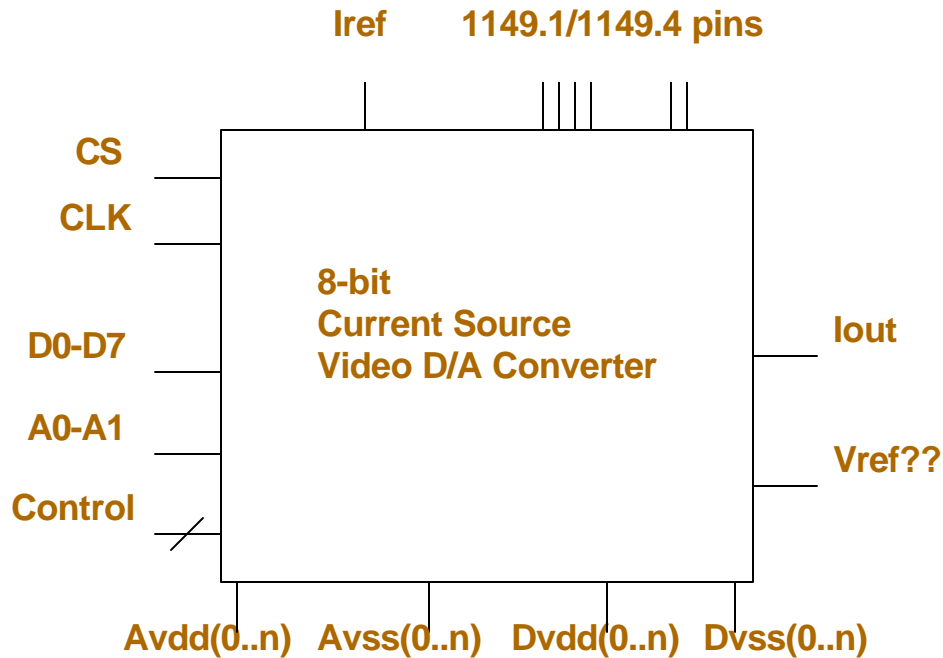


Figure 16: Video D/A System Description Pictorial

C.1.1.2 Block Diagram

The D/A converter consists of two basic arrays, a set of digital registers, and a control block. See Figure 17: Video D/A Block Diagram

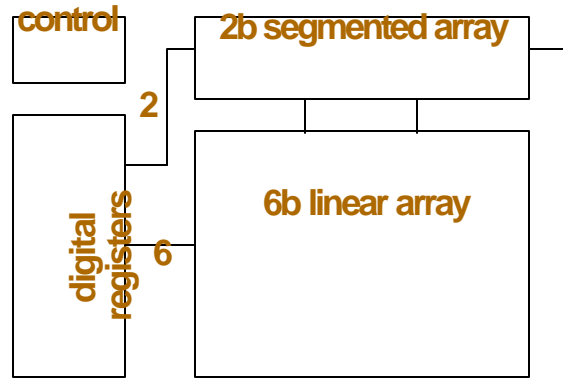


Figure 17: Video D/A Block Diagram

C.1.1.3 Register Description

There are four 8-bit wide registers in this circuit. The address inputs A0 and A1 address the registers.

A1, A0	Register	Usage
0 0	R0	Routed to analog array, normal operation
0 1	R1	Routed to analog array, assist in test
1 0	R2	controls the mode of operation
1 1	R3	unused

C.1.1.4 Timing Diagrams

Figure 18: Video D/A Timing Diagram shows the timing diagram for the circuit operation.

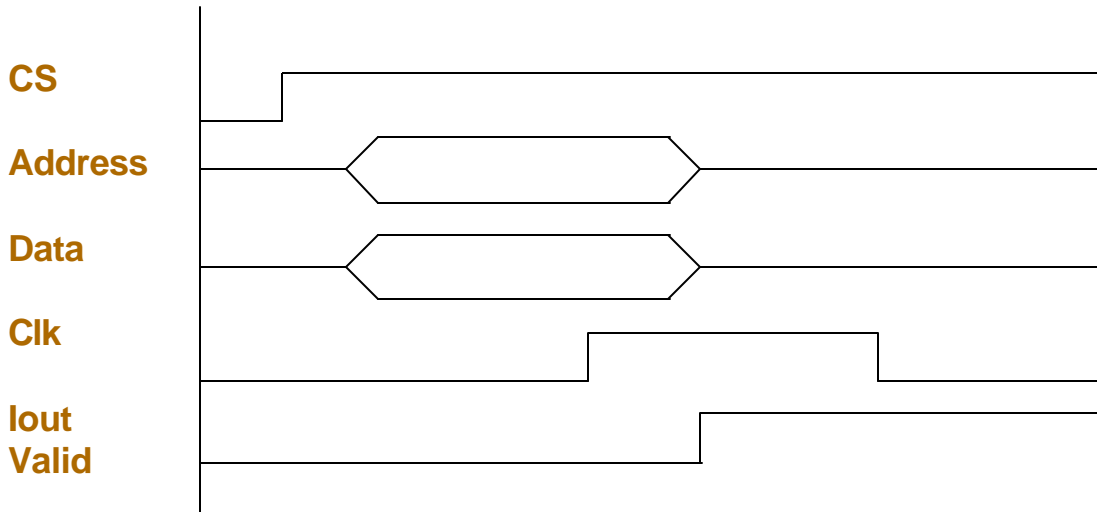


Figure 18: Video D/A Timing Diagram

C.1.1.5 Clock Distribution

The input load capacitance to this block is a minimum sized inverter. The clock is internally buffered to drive the array.

C.1.1.6 Bus Interfaces & I/O Configurations

This would contain a detailed description of how the registers work on the bus.

- Iout output range
- Voltage, current operation
- The load impedance for Iout is 75 Ohms
- Iref input range, $a \text{ mA} < I_{ref} < b \text{ mA}$

Table 3: Pin Type Information for IO Configuration

Pin	Internal	External		Test Capabilities	Guidelines
		ESD Protection	Short-Ckt Protection		
Iout	no	yes, 2kV Human Body Model	yes	yes	minimize impedance loading
...					

C.1.1.7 Test Description

Standard 1149.1 and 1149.4 pins have been added. The basic manner in which tests will be conducted is described here.

C.1.1.8 Integration Requirements

There are no special integration requirements above and beyond what has been called out by the specific deliverable items.

C.1.1.9 Schematic Block Diagrams

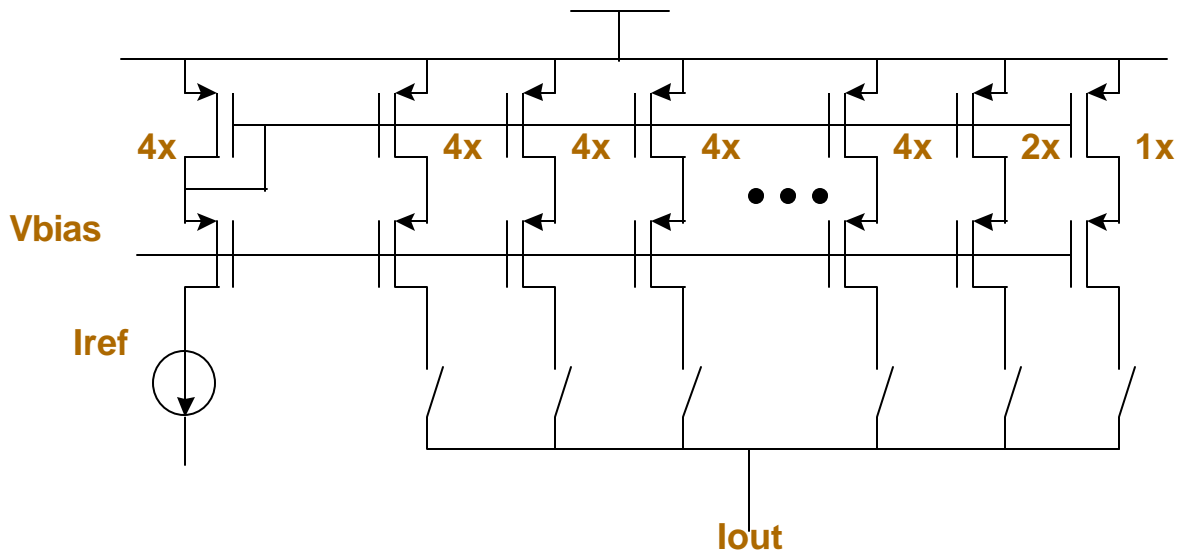


FIGURE 12. VDDO D/A SCHEMATIC BLOCK DIAGRAM

C.1.1.10 Operating Modes

- R2 sets the modes. R2=0 puts the D/A converter in standard operating mode. R2=1 sets it in switch mode where the input switches between R0 and R1. R2=2 sets it in standard test mode.
- The chip select (CS) disables the CSVC. De-asserting CS will put the CSVC in sleep mode where IDDQ testing can be done, as long as no current flows through Iref.

C.1.1.11 Bias Supply Management

An accurate I_{ref} current must be produced external to CSVC. It can be generated by a bandgap reference.

C.1.1.12 Operating ranges

The CSVC has been designed to operate between $-x^{\circ}\text{C}$ and $+y^{\circ}\text{C}$. The nominal temperature is 25°C .

C.1.1.13 Power Supplies

The CSVC is designed to operate with a 3.3V power supply. However, with slight modification by the CSVC supplier, the power supply has a range of 2.0V to 5.0V depending on the process and performance requirements.

C.1.1.14 Electrical Specifications

- See “Claims and Assumptions” for the specifics.
- The performance specifications include INL, DNL, output frequency, glitch energy, DAC settling time.
- INL would be defined here.
- Test conditions and accuracy statements.

C.1.1.15 Bonding Pad Requirements

A standard analog pad can be used for the I_{out} pin. The pads provided in this GDSII file should be used for I_{out} and A_{vdd} and A_{vss} with this VC.

C.1.2 Claims and Assumptions

- Functionality - D/A conversion function.
- Performance (measured or estimated) - The circuit can operate from 20MHz to 175MHz, and has an INL < 0.5 lsb, and a DNL < 0.5 lsb. The maximum glitch energy is xx. The D/A settling time is less than 3ns. (These are only example specifications. There are more specifications necessary for this type of converter in this application.)
- Power usage (measured or estimated) - xx mW.
- Implementation size or gates as appropriate to indicate area (measured or estimated) - xx mm² in a 0.8μ process.
- VSIA Data formats table - provided.
- Testability - supports IEEE 1149.1 and IEEE 1149.4 test bus architecture.
- Test suites and/or test streams - provided.
- These characteristics can be insured over the range of specified operating conditions.

C.1.3 Verification of Claims

The claims have been verified using a bonded out prototype. Test measurements were taken verifying the models and the performance specifications listed.

Upon delivery of the VC physical data, it is guaranteed to have undergone DRC and LVS checking. Simulation results for full CSVC circuit simulation will be provided.

C.1.4 Version History

This block has been used in a CMOS xyz 0.5μ process. The CSVC with slight modification had been used in the CMOS xyz 0.8μ and 1.0μ processes as well.

C.1.5 Known Bugs

The R3 unused register must be set to 0 when not in use. Setting it in any other mode can cause the LSB bit in the R0 register to be corrupted.

C.1.6 Application Notes

When integrating this VC, care must be taken to provide a clean power supply. Area permitting on the IC, bypass capacitors across analog V_{dd} and V_{ss} should be placed external to the VC. Board bypass capacitors should also be placed to the actual bonded out analog power pins.

C.2 Process Definition

C.2.1 Process Requirements

This D/A uses an 0.5μ CMOS process with dual-poly and dual-layer metal (minimum pitch = 1.0μ). Polysilicon resistors ($2k/sq.$) are used for biasing, and poly-poly capacitors ($.8fF/sq. \mu$) are used for frequency compensation of internal amplifiers. There is no requirement for trimming.

The first level of poly is only used for the capacitors in this VC. Since the capacitors are non-critical, this VC could also be built with a single-layer poly process with another type of capacitor.

C.2.2 Process Tolerances

The D/A has been successfully built in the Anyfab, Inc. 0.5μ process, but analysis has been done to verify that specifications could also be met with integration in similar processes from VendorX and Foundryland.

C.2.3 Process Sensitivities

This D/A is designed to operate within specifications for MOS threshold voltages of $0.7V \pm 0.15V$. The bias resistors and compensation capacitors are non-critical, and other component types can be substituted as long as the values are maintained. For example, junction resistors can be used instead of the polysilicon resistors, but the a tolerance of $\pm 20\%$ (including sheet resistance and width variation) must be met. Temperature variation must be less than $\pm 2600ppm/^{\circ}C$. Capacitor tolerance is $\pm 25\%$ for amplifier stability. The original design uses poly-poly capacitors with low bottom-plate parasitics, so re-simulation should be done if poly-over-N+ capacitors are substituted.

Matching is critically important to the linearity of the current sources. Transistor current mismatching for $50\mu/0.8\mu$ PMOS devices must be less than 1% for operation in saturated mode with $10\mu A < I_d < 50\mu A$ and $V_{ds}=1V$. This includes the combination of W/L and V_t mismatch. The DNL specification degrades linearly with current-source mismatch. For example, the DNL specification would change from 0.75LSB to 1.5LSB with current-source matching of 2%.

C.2.4 Process Design Rule Exceptions

No design rule exceptions were used in this design.

C.2.5 VC Processing History and Portability

The D/A has been successfully built in the Anyfab, Inc. 0.5μ process, but analysis has been done to verify that specifications could also be met with integration in similar processes from VendorX and Foundryland.

C.3 System Architecture and Design

C.3.1 Algorithmic Level Model

A one line equation is provided to indicate the mathematical transformation of 8 bits of information to an analog value quantized at 256 distinct levels.

Sample input and outputs are provided as well as documentation as to the rationale behind developing the model.

C.3.2 System Evaluation Model / Behavioral Model

This model describes the basic function of the D/A converter of translating an 8-bit digital code to an analog signal. It also models the performance of the block including timing, INL, and DNL. In addition, it contains the information to simulate the degradation on INL, DNL, and performance based on non-ideal connections to the VC. For example, if I_{ref} has a certain impedance, this might change the offset and gain for the D/A. A more advanced version of this model also includes the effect of substrate noise on timing, INL, and DNL.

A second model has been included in this case to accurately predict power consumption given the value of the reference current.

A test setup is included with this model as well as documentation on how it was validated.

C.3.3 Bonded Out VC / Prototype

A prototype has been designed and fabricated and is available upon request. The measured data is provided here. The output I/O pins are functionally equivalent to the I/O pins on the D/A VC. It can be used in a rapid prototyping environment.

A test set is included with this IC as well as documentation on how it was tested.

C.4 Functional and Performance Modeling

C.4.1 Digital Placeholder (“Dummy”) Model

This model, written in Verilog (could just as easily have been written in VHDL), is a pin accurate model of the D/A converter (it may be functional and cycle or timing accurate, but this is not necessary). It is very light-weight.

A test bench and documentation on how the model was developed are included.

C.4.2 Functional/Timing Digital Simulation Model

This contains a functional model of the D/A converter which accurately represents the usage of the registers, clock, and address lines. The output current is represented, but the performance of the D/A is such that it is perfectly linear.

A test bench and documentation explaining how this model was verified against more accurate models are included.

C.4.3 Digital Timing Model for Static Timing

This model contains the path delays, signal slew rates, and timing checks for the digital register of this D/A converter. As there are no state-dependent timing and modes of operation, clock networks, functional information, and support for multiple operating conditions in this D/A converter, the model does not provide information for these areas.

Included is information on how the model was validated.

C.4.4 Bus Functional Model (for digital interface)

This model is a pin accurate, timing accurate model for the register interface to the D/A converter.

Testbench and model validation information are included.

C.4.5 Peripheral Interconnect Model (for digital interfaces)

This model in the SPEF format contains the resistor and capacitor values from the register interface pins of the D/A converter.

Model validation information is included.

C.4.6 Electrical Port Models

C.4.6.1 Digital Electrical Port Model

This model contains a netlist of the interface circuits of the digital register interface for the D/A converter.

Testbench and model validation information are included.

C.4.6.2 Analog Electrical Port Model

This model contains a netlist of the analog input and output pins including I_{out} and I_{ref} .

Testbench and model validation information are included.

C.4.7 Block Level HDL Simulation Model

This model contains an implementation independent (only an example - does not necessarily have to be implementation independent) description of the digital input in Verilog, and a mixed high-level and circuit level description of the analog circuit in Verilog-A. It is accurate enough to have meaningful results for the following test bench.

Verification Test Bench

Test 1 (conservative static test):

- Set the clock at 50 MHz.
- Apply data=0 to 255.
- Measure I_{out} . INL and DNL should be close to 0, < 0.05 lsb due to systematic simulation error and minor settling time error.

Test 2 (dynamic test):

- Set the clock at 150 MHz.
- Apply data transitions, 0-1, 3-4, 7-8, 15-16, 31-32, 63-64, 127-128.
- Measure I_{out} to be certain that the DNL is less than 0.15 lsb due to settling time error.

Model Validation

The circuit simulation has been conducted to verify the high level description models in Verilog-A. The comparison is listed below. Unfortunately, due to long run-time of circuit simulation, only a few select points have been simulated to compare the models.

C.4.8 Detailed Transistor/Gate Level Schematics

A schematic has been drawn to include all of the details of this design, including W and L values for all transistors. Back annotation of critical parasitics have been included. Comments have also been included on the schematic to indicate why certain design trade-offs were made.

C.4.9 Circuit Level Simulation Netlist

This is a full transistor level netlist of the D/A converter.

Testbench and model validation information are included.

C.5 Test Requirements

This section describes the way in which the 1149.1 and 1149.4 pins are used to test the D/A. The D registers can be loaded serially via the 1149.1 pins, and the output of the D/A can be measured via one of the 1149.4 pins.

C.5.1 Signal Requirements

- The enclosed STIL file puts the VC into test mode. The pattern should be applied through the scan input.

- There are two digital signal files. The file called “static” provides a ramp signal that steps the D/A through all codes and is applied through the scan input. The file is arranged MSB first with 8 bits per word. The file called “dynamic” provides a repetitive major carry for testing glitch energy, and a zero to full scale transition for testing settling time.
- The dynamic test can only be performed if separate, parallel access is provided to the D/As inputs with sufficient bandwidth to carry the 175MHz signals. Note that serial access through the scan chain is not feasible for this test, as it would require a rate of 1400MHz to be supported.
- Testing linearity (INL, DNL) requires measurement of the D/A output level for each input code. These levels can be measured using a Voltmeter, or a digitizer.
- Testing glitch energy and settling time requires capturing at least one period of the major carry transition (01111111 to 10000000 and back) and one period of the zero-scale to full-scale transition (00000000 to 11111111 and back). High bandwidth sampling digitizers are required for glitch energy and settling time, in order to preserve high frequency components in the captured signal. An accurate amplitude measurement of 0.05% with a bandwidth of 2GHz is required.

C.5.2 Test Requirements

- A digital pattern is used to generate D/A output responses for measurement of INL, DNL, and glitch energy. For each vector driving the D/A digital input pins, the output current can be determined by measuring the dc voltage across the 75 ohm resistor.
- The “dynamic” file should be used in conjunction with a high bandwidth sampling digitizer, which is set to capture the D/A output waveforms containing the major carry and full scale transition. Glitch energy and settling time are calculated from the captured waveforms.
- Test time for INL and DNL is determined primarily by the speed of the tester’s dc voltmeter. This will determine how quickly the D/A can be stepped from one code to the next. Similarly, the input settling time of the voltmeter will swamp the D/As settling time. The VCs settling time is a tested parameter, but is expected to be in the range of 1ns.

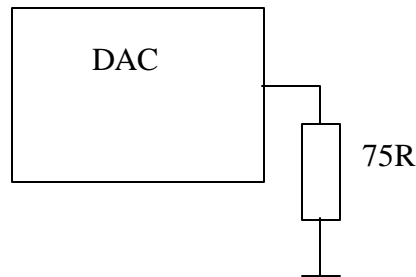


Figure 20: Example Test Setup

C.6 Physical Block Implementation

C.6.1 Detailed Physical Block Description

The detailed physical block description is provided here in the GDSII format for the VC.

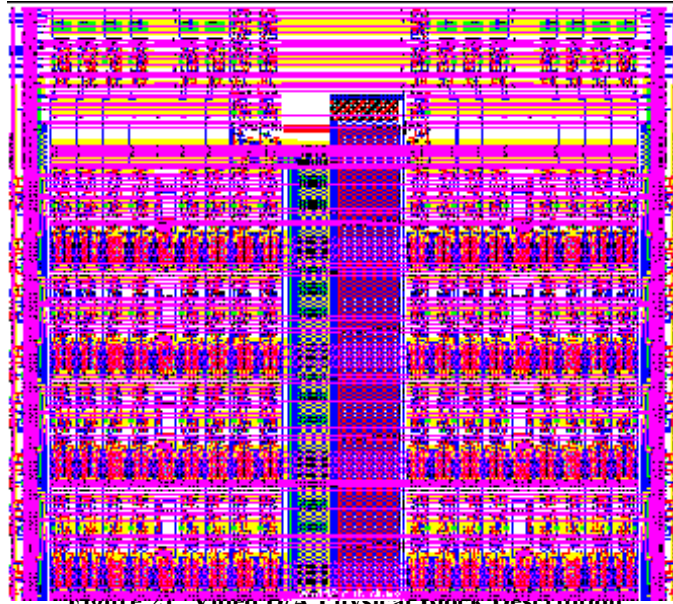


Figure 21. Video D/A Physical Block Description

C.6.1.1 Layer Mapping Table

The layer mapping table for the GDSII table is provided.

C.6.2 Pin List/ Pin Placement

This contains an abstracted view of the D/A converter which is suitable for standard place and route (special analog constraints are required, see the analog physical design information)

C.6.3 Routing Obstructions

Porosity and blockage files are provided, but essentially the rule for this VC is that only power and ground wiring can go above this. There can be no signal pins.

C.6.4 Footprint

A LEF file in VC LEF format is provided so that this VC can be automatically placed and routed.

C.6.5 Power and Ground

This section details the number of analog power pins that need to be connected given a value for I_{ref} . It also discusses how the digital power pins need to be connected and what their requirements are.

C.6.6 Physical Netlist

A netlist is provided which is sufficient for circuit simulation of the I/O circuitry. This does not contain a detailed netlist for the analog arrays nor for the internals of the digital latches. These are modeled at a high-level.

C.6.7 General Physical Rules

C.6.7.1 Physical Isolation Specification

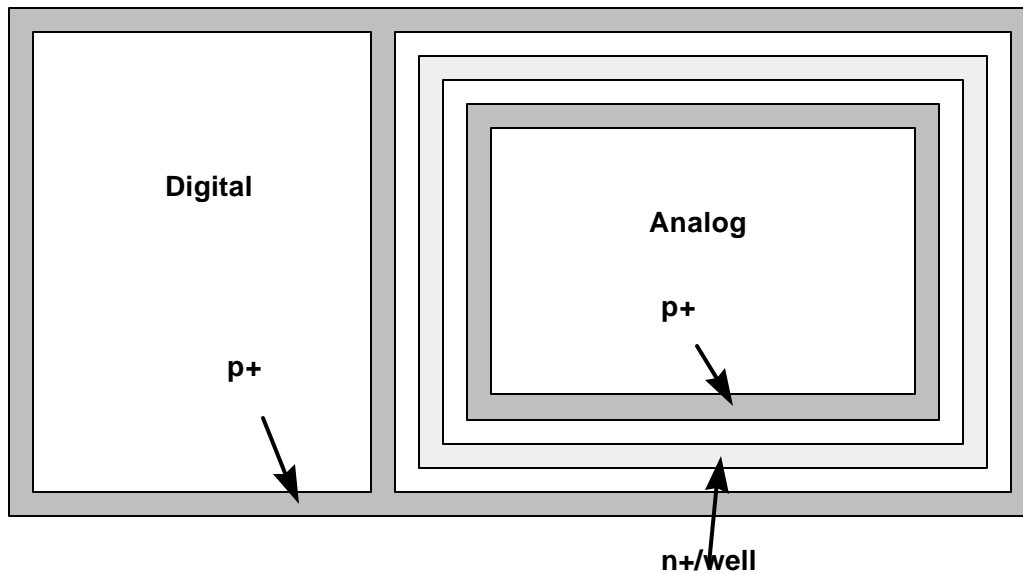


Figure 46: Physical Isolation Specification

C.6.8 Placement Specifications

C.6.8.1 Placement Constraints

This VC must reside next to the output bonding pad to which I_{out} is connected. It cannot be surrounded on 4 sides by digital circuits.

C.6.8.2 Proximity effects

This circuit will dissipate x mW. It should not be placed next to high energy consuming VCs.

C.6.9 Interconnect Specifications

C.6.9.1 Special Hookup Guidelines

The I_{out} pin must be shielded above and below to stray digital signals.

C.6.9.2 Routing Constraints

The resistance on the I_{out} pin must be less than x ohms.

C.6.9.3 Special Pin Requirements

The I_{out} pin must be next to a ground pad.

C.6.9.4 Additional Power, Ground, and Substrate Interconnect Constraints

The resistance on the analog power supplies must be less than x ohms.

C.6.10 Substrate Sensitivity/Constraints

The substrate noise on the digital circuits in the frequency band x , must be restricted to y μ A.

D. VC Delivery Example

The line items specified in the VSIA documents do not necessarily have to be shipped to a VC integrator all at once. Since analog VCs are so process dependent, when a VC integrator requests a block from a VC provider, it may take the VC provider 2 or 3 months to create that block. In such cases, the line items in the deliverables can be shipped in phases.

A possible scenario might be:

- A VC supplier may advertise with Specifications (2.1.1) and with Claims and Assumptions (2.1.2).
- When a VC integrator is interested, he may contact the VC supplier and ask for the system evaluation model (2.3.2) or the parameterized estimator for VC selection (2.1.1.14).
- The VC integrator may want more detail when the choices of VCs have been narrowed down. The VC integrator may want Verification of Claims (2.1.3) and a list of the VSI data formats and deliverables with check marks to indicate which pieces of data from Sections 2.1 to 2.6 (VSIA Data Formats and Deliverables) are available.
- The VC integrator then decides to order the part.
- The VC provider then goes through his own “black box” flow to produce the hard VCs “socketized” in the VSIA format.
- The VC provider delivers the “part” which now includes all of the line items of the VSI.
- The VC integrator then takes the VC and embeds it into his system-on-a-chip.

See the VSIA Virtual Component Transfer (VCT) Development Working Group specifications for more information.

E. Future Issues

The following items have been identified as unresolved issues:

- Need a way to track process variations through a design.
- Need parameters for noise margins.
- On-chip ground instability issues.
- 50 ohms is a standard for inter-chip communication of signals on a system board. A more suitable new electrical standard for intra-chip communication may need to be defined.
- Format undefined in this document may be defined in future revisions.
- A VSIA standard addressing parameterizable analog/mixed signal virtual components may be considered.

F. Glossary of Acronyms

The acronyms listed here are in addition to those listed in the VSIA Architecture Document, Version 1.0.

A/D	Analog-to-Digital (converter)
CP	Charge Pump
D/A	Digital-to-Analog (converter)
DEF	Design Exchange Format
DNL	Differential Non-linearity
DRC	Design Rule Check
DSP	Digital Signal Processor
GCF	General Constraint Format
IDDQ	Idd Quiescent
INL	Integral Non-linearity
I/O	Input/Output
IP	Intellectual Property
LEF	Library Exchange Format
LVS	Layout vs. Schematic
OTA	Operational Transconductance Amplifier
PLL	Phase-Locked Loop
SR	Shift Register
STIL	Standard Test Interface Language
TTM	Time-To-Market
VC	Virtual Component
VCO	Voltage Controlled Oscillator
VSI	Virtual Socket Interface

G. Bibliography

- [1] R. Neff, Ph.D. Thesis, Electrical Engineering and Computer Sciences, University of California, Berkeley, 1995.
- [2] *VSI Alliance Architecture Document*, Version 1.0.
- [3] H. Chang, "Analog IP Critical for System Design," *Electronic Engineering Times*, 3/29/99, page 80.

